# Device applications of the giant direct and inverse spin Hall effect in **BiSb** topological insulator

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#### **ABSTRACT**

BiSb is a topological insulator with high electrical conductivity and a giant spin Hall effect at room temperature, making it a promising candidate for various spin-orbit torque (SOT) device applications. Over the past five years, we have demonstrated proof-of-concept of physical vapor deposition of high quality BiSb thin film, integration of BiSb perpendicularly magnetized ferromagnetic multilayers with high electrical conductivity ( $\sim 1.5 \times 10^5 \,\Omega^{-1} \text{m}^{-1}$ ) and a giant spin Hall angle (> 10), ultralow current ( $10^4 \sim 10^5 \,\text{A/cm}^2$ ) and ultrafast (~1 ns) switching of ferromagnetic multilayers by BiSb, integration of BiSb to CoFeB/MgO/CoFeB-based magnetic tunnel junction with relatively high tunneling magnetoresistance ratio and low switching current density. For practical device applications, we have collaborated with storage vendors such as SamSung and Western Digitals to develop several fundamental technologies utilizing the giant spin Hall effect of BiSb for high-level SOT-MRAM cache memory and SOT magnetic sensing device for read head sensor in hard disk drive. We show that BiSb-integrated SOT magnetic sensor has a giant inverse spin Hall angle (~61), which is good enough for use in 4 Tbit/inch<sup>2</sup> magnetic recording technology. Furthermore, we demonstrated that BiSb after 400°C annealing and recrystallization can still have high enough spin Hall angle for ultralow current switching in SOT-MRAM. Our works open the way for SOT device applications of BiSb topological insulator.

Keywords: Topological insulator, BiSb, SOT-MRAM, SOT sensor

# 1. INTRODUCTION

Magnetic and spintronic devices are at the forefront of innovative ultralow power technologies that are revolutionizing the electronic, healthcare, and energy sectors. Emerging spintronic phenomena, such as the spin Hall effect (SHE) and the associated spin-orbit torque (SOT), hold great promise for driving significant advancements in high-performance magnetic sensors, next-generation memory, and energy-efficient artificial intelligence devices. Our research group and others in the field have been investigating various materials that can effectively harness the spin Hall effect for these applications. Notable materials include topological insulator (TI) materials such as Bi<sub>2</sub>Se<sub>3</sub> [1,2], (Bi,Sb)<sub>2</sub>Te<sub>3</sub> [3]. Bi<sub>1-x</sub>Sb<sub>x</sub> with  $0.07 \le x$  $\leq$  0.22 [4], as well as topological semimetal (TSM) such as YPtBi [5,6,7] which exhibit strong spin-orbital coupling (SOC). The strength of the SOC is represented by the spin Hall angle (SHA)  $\theta_{SH}$ , which is given by  $\theta_{SH} = \frac{2e}{\hbar} \frac{J_s}{J_c}$ ,

$$\theta_{\rm SH} = \frac{2e}{\hbar} \frac{J_{\rm s}}{J_{\rm c}}$$
,

where  $J_{\rm S}$  and  $J_{\rm C}$  are the charge and spin current density, respectively. Among all the TI and TSM materials, we identify BiSb as the most suitable choice for device applications due to its distinctive band structure and multiple topological surface states (TSS) [8]. These TSS exhibit gapless metallic Dirac cones, which serve as monopoles of the Berry phase curvatures in momentum space [9], thereby enhancing charge-to-spin conversion efficiency and surface conductivity. Theoretically and experimentally findings indicate that BiSb has varying numbers of Dirac cones depending on its crystal orientations: (012) and (001). Here, we use the hexagonal coordinate indexing for  $Bi_{1-x}Sb_x$ . The surface conductivity of thin BiSb films is significantly more critical than that of the bulk, particularly for high-performance SOT applications, such as SOT magnetic sensors [10, 11] or ultrafast and low-power SOT-MRAM devices [12,13,14]. In the (012) orientation, BiSb possesses four Dirac cones [15] contrasting with the single Dirac cone found in the (001) orientation [16], thus making the (012) orientation the preferred choice for achieving a higher magnitude of the spin Hall angle. These characteristics position BiSb as a promising candidate for low-power consumption devices. However, the growth of BiSb film stacks in the (012) orientation, along with the need to ensure their thermal stability, presents challenges for the commercial application of BiSb materials in SOT devices. This is particularly significant since BiSb has predominantly been grown using the molecular beam epitaxy technique on GaAs(111)A [17,18], Si(111) [19], and BaF<sub>2</sub> [20]. It is critical

to explore growth methods of high quality BiSb using the physical vapor deposition (PVD) technique while maintaining device performance and reliability. To address this challenge, we first explored epitaxial growth of BiSb(001) on sapphire substrate using the PVD, and then epitaxial or highly textured growth of BiSb in the (012) orientation on more practical Si/SiO<sub>x</sub> substrates. Then, we demonstrated integration of BiSb / perpendicularly magnetized ferromagnetic multilayers with high electrical conductivity ( $\sim 1.5 \times 10^5~\Omega^{-1} \text{m}^{-1}$ ) and a giant spin Hall angle (> 10) [21], ultralow current ( $10^4 \sim 10^5~\text{A/cm}^2$ ) [22], ultrafast ( $\sim 1~\text{ns}$ ) switching of ferromagnetic multilayers by BiSb [12], integration of BiSb to CoFeB/MgO/CoFeB-based magnetic tunnel junction [13] with relatively high tunneling magnetoresistance ratio and low switching current density. For practical device applications, we have collaborated with storage vendors such as SamSung and Western Digitals to develop several fundamental technologies utilizing the giant spin Hall effect of BiSb for highlevel SOT-MRAM cache memory and SOT magnetic sensing device for read head sensor in hard disk drive. We showed that BiSb-integrated SOT magnetic sensor has a giant inverse spin Hall angle ( $\sim 61$ ), which is good enough for use in 4 Tbit/inch² magnetic recording technology. Furthermore, we demonstrated that BiSb after 400°C annealing and recrystallization can still have high enough spin Hall angle for ultralow current switching in SOT-MRAM. Our works open the way for SOT device applications of BiSb topological insulator.

# 2. GROWH OF HIGH QUALITY BISB BY PHYSICAL VAPOR DEPOSITION

The giant spin Hall effect was first observed in molecular beam epitaxy-grown BiSb(012)/MnGa bilayer [4], where the spin Hall angle  $\theta_{\rm SH}$  is as high as 52. However, for realistic device application, high quality BiSb must be grown by PVD. We first demonstrated deposition of BiSb thin films with various thicknesses on sapphire C-plane (0001) substrates by radio-frequency magnetron sputtering from a single  $Bi_{0.85}Sb_{0.15}$  target [23]. Since the lattice constants are a = 4.51 Å, c =11.8 Å for  $Bi_{0.85}Sb_{0.15}$  and a = 4.76 Å, c = 13.0 Å for sapphire, there is an in-plane lattice mismatch of -5.3% between BiSb and the sapphire substrates. The samples were deposited by either Ar or Kr plasma. For 10 nm-thick BiSb films, we found that the substrate temperature  $T_S = 50^{\circ}$ C was optimal, as for  $T_S$  higher than 100°C, the films became nonconductive due to island growth. On the other hand, the best  $T_S$  for films over 14 nm was 150°C. To further improve the crystal quality, we employed a two-step technique for thick films. First, we deposited a BiSb layer thinner than 10 nm at 50°C. Then, we increased  $T_{\rm S}$  to 150°C, and annealed the layer for 10 minutes. Finally, we deposited the rest at 150°C. We found that this two-step technique can improve the crystal quality and the electrical conductivity of BiSb thin films thicker than 10 nm.  $\theta$ -2 $\theta$  X-ray diffraction (XRD) spectra of 10 nm-thick BiSb thin films show no other phase than BiSb(001), demonstrating that it is possible to obtain a single-phase BiSb thin film by sputtering deposition. As the thickness increases, extra phases such as BiSb(012) and BiSb(014) start to appear. Meanwhile, the two-step deposition can significantly suppress these extra phases. Indeed, the BiSb(001) single phase was observed up to at least 24 nm by the two-step deposition. For samples deposited by Kr plasma, the BiSb(001) single phase was observed even by one-step deposition up to 50 nm. The surface morphology observed by atomic force microscopy shows that the 10 nm thick BiSb films have smoother surfaces than thicker films. The roughness of 10 nm-thick BiSb thin films is about  $0.8 \sim 0.9$  nm. However, the surface smoothness deteriorates rapidly as the thickness increases from 10 nm, which is consistent with the emergence of other phases as revealed by the XRD spectra. We then performed the XRD  $\chi$  (tilting angle) –  $\varphi$  (azimuth angle) scan to investigate the inplane texture of the 10 nm-thick samples A and K deposited by Ar or Kr gas, respectively. The  $\theta$  angle was set at 13.6° for the (012) plane. Figure 1(a) and 1(b) show the polar mapping for  $\chi = 0.90^{\circ}$  and  $\varphi = 0.360^{\circ}$  scan of samples A and K, respectively. The polar maps show 6 strong peaks located at  $\chi = 55^{\circ}$ . Considering the epitaxial single crystal BiSb(001) has 3 distinct peaks at  $\chi = 55^{\circ}$  separated by the azimuth angle of 120°, Figs. 1(a) and 1(b) indicate that there are equivalent twin crystals in samples A and K [24,25]. However, there is no other plane in the polar maps besides BiSb(012), indicating the high crystal ordering of sputtered BiSb films despite the large in-plane lattice mismatch of -5.3% between the BiSb films and the sapphire substrates. We further characterize the crystal structure at the interface between BiSb and the sapphire substrates by using high-resolution transmission electron microscopy (TEM). Figure 1(c) shows a TEM image of a BiSb film deposited on sapphire by Ar plasma, magnified near the interface. One can see that the first 2 nm BiSb has some crystal disorder, which absorbs the lattice mismatch with the sapphire substrate. When the thickness exceeds 2 nm, the crystal ordering improves rapidly, and an epitaxial BiSb film can be obtained. These results show the robustness of BiSb against lattice mismatch.

Another distinct feature of BiSb from other well-known V-VI TIs such as Bi<sub>2</sub>Se<sub>3</sub>, Bi<sub>2</sub>Te<sub>3</sub> or Sb<sub>2</sub>Te<sub>3</sub>, is that its bulk is always an intrinsic semiconductor with the Femi level in the band gap. This is because Bi and Sb are in the same V-group, thus deviation of the composition or existence of anti-site defects does not result in any donors / acceptors that would generate free carriers and shift the Fermi level to the conduction band (as in the case of Bi<sub>2</sub>Se<sub>3</sub> or Bi<sub>2</sub>Te<sub>3</sub> due to anti-site Se/Te) or

to the valence band (as in the case of Bi<sub>2</sub>Te<sub>3</sub> or Sb<sub>2</sub>Te<sub>3</sub> due to anti-site Bi/Sb). This intrinsic semiconducting behavior of the bulk states has been confirmed in MBE-grown BiSb films on GaAs(111)A substrates. Thus, the temperature dependence of the bulk conductivity is given by  $\sigma_{\rm B} = \sigma_{\rm B0} \exp\left(-\frac{E_{\rm g}}{2k_{\rm B}T}\right)$ , where  $E_{\rm g}$  is the effective band gap,  $k_{\rm B}$  is the Boltzmann constant, and T is the temperature. Therefore, the total conductivity can be described by [26],

$$\sigma = \sigma_{\rm Sh}/t + \sigma_{\rm B0} \exp\left(-\frac{E_{\rm g}}{2k_{\rm B}T}\right) \tag{1},$$

where  $\sigma_{\rm Sh}$  is the surface sheet conductivity.

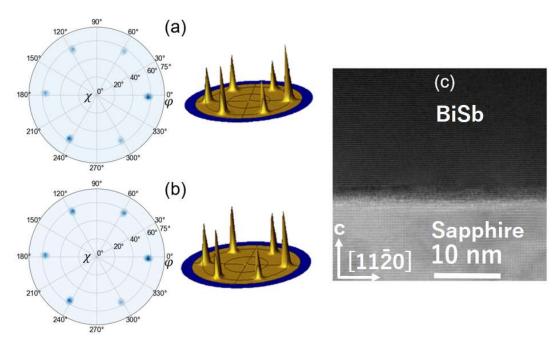


Figure 1. (a)(b) XRD  $\chi$ - $\varphi$  polar mapping of the 10 nm-thick BiSb films deposited by Ar and Kr plasma in one-step, respectively. (c) TEM image near the interface of BiSb (001) /sapphire C-plane (0001) substrate. Reprinted from Ref. [23] with permission from IOP publishing.

We measured the temperature dependence of resistivity in order to further demonstrate the existence of the surface states. Figures 2(a)-2(d) show the temperature-dependence of the electrical resistivity normalized by its value at 300 K ( $\rho/\rho_{RT}$ ) for Ar one-step, Ar two-step, Kr one-step, and Kr two-step samples, respectively. For thick samples, there are parallel conduction on the surface and in the bulk due to thermally excited intrinsic carriers at room temperature. With the temperature decreasing, the bulk conduction is suppressed, and the surface conduction becomes overwhelmingly dominant, explaining the plateaus of resistivity below 100 K observed for thick samples in Figs. 2(a)-2(d). The dashed lines in Figs. 2(a)-2(d) are fits to the experimental data using equation (1). For 10 nm-thick samples, the surface conduction dominates even at room temperature, thus the resistivity is nearly temperature-independent, confirming the metallic nature of the surface states [26]. These behaviors are similar to those of high quality MBE-grown BiSb thin films. These results show that it is possible to grow high-quality BiSb thin films by the industry-friendly PVD technique.

Next, we explored epitaxial or highly textured growth of BiSb in the (012) orientation on more practical Si/SiO<sub>x</sub> substrates [27]. We found that 4-fold and 3-fold symmetric seed layers can significantly enhance the growth of Bi<sub>0.9</sub>Sb<sub>0.1</sub> in the (012) orientation. The lattice structure of BiSb (012) exhibits an almost cubic configuration, with in-plane dimensions of a = 4.54 Å and b = 4.74 Å. This nearly square lattice arrangement facilitates efficient (012) growth on both 4-fold symmetric single-crystal substrates and (100) cubic or (001) tetragonal textured seed layers. Furthermore, Bi<sub>0.9</sub>Sb<sub>0.1</sub>(012) can be grown on 3-fold symmetric (111) seed layers. Particularly, undoped Bi<sub>1-x</sub>Sb<sub>x</sub> has a squarer (012) surface, which facilitates the epitaxial growth of Bi<sub>1-x</sub>Sb<sub>x</sub> on cubic-textured (100) or tetragonal (001) seed layers. Meanwhile, the doped BiSb:X, where X is a dopant, has a more rectangular (012) surface. Thus, a highly textured (012) Bi<sub>1-x</sub>Sb<sub>x</sub>:X with more rectangular surface can be grown on a seed layer composed of (111) polycrystalline material or, alternatively, nanocrystalline or amorphous materials, depending on the matching between the rectangular Bi<sub>1-x</sub>Sb<sub>x</sub>(012) surface and the (111) rectangular surface

formed by two or more adjacent hexagons in a long-range polycrystalline (111) fcc surface or local clusters of hexagons from nanocrystalline or amorphous materials that create a pseudo-crystalline (111) surface. In fact, we demonstrated the growth of highly textured  $Bi_{0.9}Sb_{0.1}:N(012)$  (100 Å) on the nanocrystalline NiFeGe(111) interlayer (12 Å), which itself was deposited on top of a CoFe (7 Å) ferromagnetic (FM) layer. Meanwhile, a stack consisting of NiFeGe (27 Å) /RuX (20 Å) or NiFeTa (15 Å) / RuX (20 Å), a conditioning layer (18 Å) can be utilized to grow epitaxial non-doped  $Bi_{0.9}Sb_{0.1}$  (120 Å) TI layer. Here, the RuX plays the role of a (100) cubic seed layer, and the conditioning layer transfers the (100) cubic surface to BiSb(012) while preventing interaction between BiSb and the RuX layer. All of these stacks show strong BiSb(012) orientation with relatively low surface roughness (~10 Å) and high spin Hall angle ~ 10 for the as-grown films. These results indicate that it is possible to grow a high quality BiSb layers with excellent spin Hall performance on  $Si/SiO_x$  substrate, opening the possibility of utilizing the giant spin Hall effect of BiSb for high-performance SOT devices.

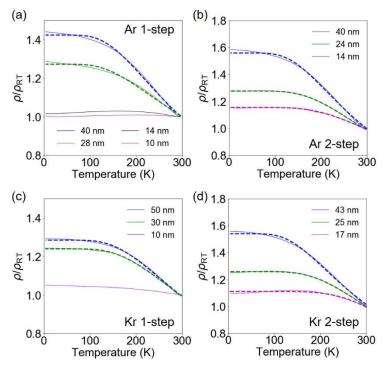


Figure 2. Temperature dependence of normalized resistivity  $\rho/\rho_{RT}$  of BiSb films deposited by (a) Ar plasma in one-step, (b) Ar plasma in two-step, (c) Kr plasma in one-step, and (d) Kr plasma in two-step. Dashed lines are fitting using Eq. (1). Reprinted from Ref. [23] with permission from IOP publishing.

#### 3. BISB / FERROMAGNETIC MULTILAYERS FOR SOT-MRAM APPLICATION

For TI being a practical material for SOT-MRAM, the following three minimum requirements must be satisfied: (1) a large spin Hall angle of the order of 10, (2) large electrical conductivity  $\sigma$  of order of  $10^5 \Omega^{-1} \text{ m}^{-1}$ , and (3) can be deposited using sputtering deposition. The first two requirements are for optimization of the switching current density and switching energy. We first demonstrated high spin Hall angle, high electrical conductivity, and efficient SOT switching by BiSb in fully sputtered BiSb – (Co/Pt) multilayers with large perpendicular magnetic anisotropy (PMA) on sapphire substrate [21]. In this stack, the BiSb layer was deposited on top of the Co/Pt multilayers (i.e. top SOT). We show that the sputtered BiSb has a large spin Hall angle of  $\theta_{\text{SH}} = 10.7$  and high electrical conductivity of  $\sigma = 1.5 \times 10^5 \Omega^{-1} \text{m}^{-1}$ , thus satisfying all the three requirements for SOT-MRAM implementation. Despite the large PMA field of 5.2 kOe of the (Co/Pt) multilayers, we achieve robust SOT magnetization at a low current density of  $1.5 \times 10^6 \text{ A/cm}^2$ . Table 1 summarizes  $\theta_{\text{SH}}$ ,  $\sigma$ , the spin Hall conductivity  $\sigma_{\text{SH}}$ , and the SOT normalized power consumption  $P_n$  at room temperature of several heavy metals and TIs. Here,  $\theta_{\text{SH}}$  of TIs are their best values reported in literature. For the calculation of the  $P_n$ , we assumed bilayers of spin Hall material (thickness t = 6 nm for heavy metals and t = 10 nm for TIs) and CoFeB (thickness  $t_{\text{FM}} = 1.5$  nm, conductivity  $\sigma_{\text{FM}} = 6 \times 10^5 \Omega^{-1} \text{ m}^{-1}$ ). Considering the shunting current in the ferromagnetic layer, the SOT power consumption is

proportional to  $(\sigma t + \sigma_{FM}t_{FM})/(\sigma t\theta_{SH})^2$ . One can see that not only  $\theta_{SH}$  but also  $\sigma$  affect the SOT power consumption, a fact usually overlooked in literature. For example, while the sputtered  $Bi_xSe_{1-x}$  has a much larger spin Hall angle  $(\theta_{SH} = 18.6)$  than that  $(\theta_{SH} = 3.5)$  of MBE-grown  $Bi_2Se_3$ , their power consumption is nearly the same, because  $Bi_xSe_{1-x}$  has poorer crystal quality than  $Bi_2Se_3$  and thus very low conductivity. Meanwhile, the sputtered BiSb thin film in this work shows both high  $\sigma = 1.5 \times 10^5 \,\Omega^{-1} \,\mathrm{m}^{-1}$  and large  $\theta_{SH} = 10.7$ , which are optimal for both small switching current density and small switching power consumption [28]. Indeed, the switching power consumption for sputtered BiSb is 50 times smaller than that for sputtered Bi\_xSe\_{1-x}, and over 300 times smaller than that for W, which is the most used heavy metal in SOT-MRAM development. The small switching current density and switching power also help suppress failure of the spin Hall layer due to electromigration and Joule heating [29]. Our results demonstrate the feasibility of BiSb for not only ultralow power SOT-MRAM but also other SOT-driven spintronic devices, such as race-track memories [30] and spin Hall oscillators [31,32].

Table 1. Spin Hall angle  $\theta_{SH}$ , electrical conductivity  $\sigma_s$ , spin Hall conductivity  $\sigma_{SH}$ , and SOT normalized power consumption  $P_n$  of several heavy metals and topological insulators.

SOT Materials	$  heta_{\sf SH} $	$\sigma$ ( $\Omega^{\text{-1}}$ m <sup>-1</sup> )	$ \sigma_{SH} $ [( $\hbar/2e$ ) $\Omega^{\text{-1}}m^{\text{-1}}$ ]	<b>P</b> <sub>n</sub>
Та	0.15	5.3×10 <sup>5</sup>	8.0×10 <sup>4</sup>	1
Pt	0.08	4.2×10 <sup>6</sup>	3.4×10 <sup>5</sup>	3.6×10 <sup>-1</sup>
W	0.4	4.7×10 <sup>5</sup>	1.9×10 <sup>5</sup>	1.6×10 <sup>-1</sup>
(Bi <sub>0.07</sub> Sb <sub>0.93</sub> ) <sub>2</sub> Te <sub>3</sub> (MBE)	2.5	1.8×10 <sup>4</sup>	4.5×10 <sup>4</sup>	3.0×10 <sup>-1</sup>
Bi <sub>2</sub> Se <sub>3</sub> (MBE)	3.5	5.7×10 <sup>4</sup>	2.0×10 <sup>5</sup>	2.1×10 <sup>-2</sup>
Bi <sub>x</sub> Se <sub>1-x</sub> (Sputtered)	18.6	7.8×10 <sup>3</sup>	1.5×10 <sup>5</sup>	2.6×10 <sup>-2</sup>
Bi <sub>0.85</sub> Sb <sub>0.15</sub> (Sputtered)	10.7	1.5×10 <sup>5</sup>	1.6×10 <sup>6</sup>	5.2×10 <sup>-4</sup>

We then studied SOT magnetization switching induced by a Bi<sub>0.85</sub>Sb<sub>0.15</sub> topological insulator layer in both thermal activation and fast switching regime with pulse width down to 1 ns [12]. Figure 3(a) shows the schematic structure of the sample, which consists of (from top to bottom) Bi<sub>0.85</sub>Sb<sub>0.15</sub>(10 nm)/[Pt(0.4 nm)/Co(0.4 nm)]<sub>2</sub>/insulating buffer deposited on Si/SiO<sub>x</sub> substrates at room temperature. The BiSb layer's electrical conductivity is  $\sigma = 1.0 \times 10^5 \,\Omega^{-1} \text{m}^{-1}$  and the spin Hall angle is  $\theta_{SH} = 3.2$  as estimated from the second harmonic Hall measurement. We performed ultrafast SOT switching with pulse widths  $\tau = 1 \sim 4$  ns in a 1000 nm  $\times$  800 nm Hall bar device shown in Fig. 3(b). Figures 3(c) – 3(f) show the SOT switching loops in the fast switching regime with various  $\tau = 1 \sim 4$  ns. Figure 3(b) summaries  $J_{\rm th}^{\rm BiSb}$  as a function of  $\tau$  from 1 ms down to 1 ns at  $H_x = 1$  kOe, averaged for up-to-down and down-to-up magnetization switching. There are clearly two different regimes: the thermal activation regime ( $\tau > 10$  ns) when  $J_{\rm th}^{\rm BiSb}$  changes slowly, and the fast switching regime  $(\tau < 10 \text{ ns})$  when  $J_{\text{th}}^{\text{BiSb}}$  changes rapidly. The red dashed line is fitting by the thermal activation model, for which we found the zero-K switching current density  $J_{\rm th0}^{\rm BiSb} = 2.5 \times 10^6$  A/cm<sup>2</sup> and thermal stability factor  $\Delta = 35$ , which is nearly the same as  $\Delta \sim 38$  in CoFeB/MgO. The green dashed line is fitting for the fast switching regime by  $J_{\rm th0}^{\rm BiSb} = J_{\rm th0}^{\rm BiSb} + Q/\tau$ , which yields  $J_{\text{th0}}^{\text{BiSb}} = 4.1 \times 10^6 \,\text{A/cm}^2$  and an effective charge density parameter  $Q = 15 \times 10^{-9} \,\text{C/cm}^2$ . Although the latter model estimates  $J_{\text{th0}}^{\text{BiSb}}$  twice that of the former model, the  $J_{\text{th0}}^{\text{BiSb}}$  value is still much smaller than those observed in Co/Pt  $(J_{\text{th0}}^{\text{Pt}} \sim 0.8 \times 10^8 \,\text{A/cm}^2)$  [33], MgO/CoFeB/W  $(J_{\text{th0}}^{\text{W}} \sim 2.0 \times 10^8 \,\text{A/cm}^2)$  [34], and MgO/CoFeB/Ta  $(J_{\text{th0}}^{\text{Ta}} \sim 3.0 \times 10^8 \,\text{A/cm}^2)$  [35], estimated from the thermal activation model. These results consolidate the advantage of BiSb topological insulator for ultralow power and fast switching SOT-MRAM. We also demonstrated very small switching current density in top BiSb/ferrimagnet CoTb deposited on Si/SiO<sub>x</sub>, where the switching current can be as low as  $7 \times 10^4$  A/cm<sup>2</sup> for DC and 2.2  $\times$  10<sup>6</sup> A/cm<sup>2</sup> for 10 ns pulse current owing to the low magnetization of CoTb and the high spin Hall angle of BiSb, the formal is among the smallest SOT switching current reported so far [22].

It is more challenging to achieve a high spin Hall angle in SOT-bottom BiSb/perpendicularly magnetized FM structure, when the thickness of the FM layer is comparable to the surface roughness of bottom BiSb. To achieve a large  $\theta_{SH}$  in bottom BiSb, it is essential to insert an interlayer to block Sb diffusion from BiSb to the FM layer. We found that a Ti (3 nm) can significantly enhance the effective  $\theta_{SH}$  in bottom BiSb/Ti/Ta/CoFeB/MgO heterojunctions up to  $\theta_{SH} \sim 6$  [36]. However, Ti is metallic and can shunt the in-plane current. Thus, we have collaborated with Samsung to develop an oxide

CrO<sub>x</sub> interlayer with high resistance, for which BiSb/CrOx/Ta/CoFeB shows relatively good  $\theta_{SH} \sim 2.8$  [37]. SOT switching of CoFeB by BiSb by low DC and pulse currents were demonstrated in BiSb/interlayer/perpendicularly magnetized CoFeB. Since the BiSb layers in those stacks have a high conductivity of  $\sigma = 1.3 \times 10^5 \sim 1.5 \times 10^5 \,\Omega^{-1} \text{m}^{-1}$  and a relatively high  $\theta_{SH} = 2.8 \sim 6$ , the SOT switching power consumption is several orders of magnitude lower than those of heavy metals.

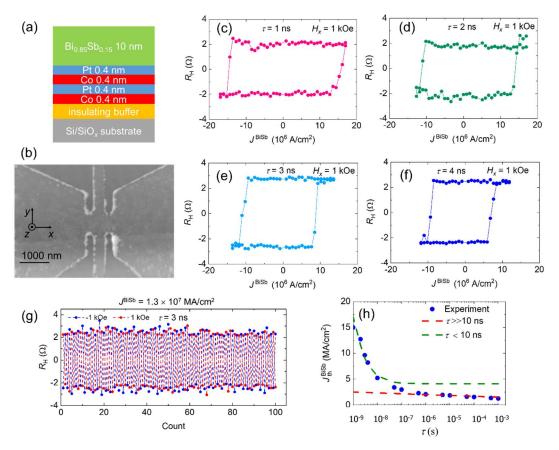


Figure 3. (a),(b) Schematic structure and image of 1000 nm × 800 nm Hall bar device consisting of Bi<sub>0.85</sub>Sb<sub>0.15</sub>(10 nm)/[Pt(0.4 nm)/Co(0.4 nm)]<sub>2</sub>/insulating buffer deposited on a Si/SiO<sub>x</sub> substrate for ultrafast SOT switching. (c)–(f) SOT switching loops of the small Hall bar device at various  $\tau$  from 1 ns to 4 ns and  $H_x$  = 1 kOe. (g) Deterministic SOT multiple switching by  $J_{\text{th}}^{\text{BiSb}}$  = ±1.3 × 10<sup>7</sup> A/cm<sup>2</sup>,  $\tau$  = 3 ns, and  $H_x$  = ±1 kOe. (h) Threshold switching current density  $J_{\text{th}}^{\text{BiSb}}$  as a function of  $\tau$  at  $H_x$  = 1 kOe. The red dashed line is fitting by the thermal excitation model ( $\tau$  >> 10 ns), and the green dashed line is fitting for the fast switching regime.

Our collaboration with Western Digital results in a hybrid interlayer consisting of metallic NiFeGe and insulating MgO for enhancing the effective spin Hall angle of BiSb [38]. The hybrid interlayer has two roles. First, it blocks interlayer atomic diffusion and protects the topological surface states to enhance the intrinsic spin Hall angle. Second, it increases the interface spin transparency by reducing the spin diffusion time across the interlayer and the spin flip/spin-transfer time at the interlayer/FM interface. Combining the epitaxial BiSb(012) grown on cubic seed layers and the hybrid buffer layer yields a high effective  $\theta_{SH} \sim 10$  for as-grown films and  $\theta_{SH} \sim 23$  for films subjected to annealing at 215°C for 3 hours [27].

We also collaborated with the K. Wang group at UCLA to integrate BiSb to CoFeB/MgO/CoFeB magnetic tunnel junction (MTJ) [13]. Figure 4(a) shows the *R-H* curve for the all sputtered BiSb(10 nm) /Ru(5 nm)/CoFeB(2.5 nm)/MgO(2 nm)/CoFeB(5 nm) three terminal device, while the Fig. 4(b) shows the current-driven SOT switching in the all sputtered BiSb-MTJ with size of 1  $\mu$ m  $\times$  3  $\mu$ m. We achieved relatively high tunneling magnetoresistance ratio  $\sim$  90% and a low switching current density  $\sim$  1.4  $\times$  10<sup>6</sup> A cm<sup>-2</sup>, demonstrating the feasibility of BiSb-integrated SOT-MRAM.

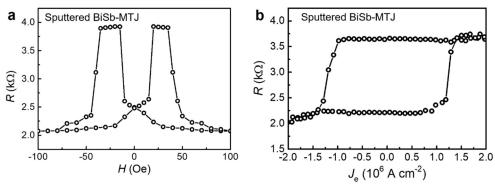


Figure 4. (a) R-H curve for the all sputtered BiSb-MTJ device. (b) Current-driven SOT switching in the all sputtered BiSb-MTJ device (1  $\mu$ m  $\times$  3  $\mu$ m).

Finally, we also studied the spin Hall effect in BiSb melted at 400°C and recrystallized. We demonstrated that BiSb with proper capping can withstand 400°C annealing and can still have high enough spin Hall angle for ultralow current switching in SOT-MRAM. Furthermore, we observed the giant spin Hall angle in BiSb up to ambient temperature of 125°C, demonstrating the capability of BiSb for high temperature applications [39].

### 4. BISB / FERROMAGNETIC MULTILAYERS FOR SOT SENSOR APPLICATION

Another important application of the giant spin Hall effect (both direct and inverse) in BiSb is the SOT sensor for ultrahigh density magnetic recording (4 Tbit/inch²) [10,11]. The structure of SOT reader consists of two layers in minimum: a ferromagnetic (FM) layer and a SOT layer, as schematically shown in Fig. 5. When applying a charge current between the top shield and the bottom shield, a perpendicular spin-polarized current is injected from the FM layer to the SOT layer. The spin polarization direction depends on the magnetization of the FM layer which senses the media stray magnetic field. The SOT layer converts the perpendicular spin-polarized current to an in-plane charge current and generates an output voltage between the two lead terminals via the inverse spin Hall effect [40]. The SOT reader requires only a single FM layer, thus it does not suffer the dimensional constrain due to the magnetic reference layer as in the case of TMR reader, making it much easier for reducing the total thickness. Furthermore, there is no spin transfer torque noise in SOT reader. However, the output voltage in heavy metal-based devices is of the order of  $\mu$ V, which is too small for SOT reader application [41] due to the relatively small spin Hall angle ( $\theta_{SH}$ ) of heavy metals. To improve the output voltage and SNR, it is essential to use a SOT material with a giant  $\theta_{SH}$ . BiSb is best fit for this application thanks to its high spin Hall angle and it can be deposited by PVD tools. We conducted theoretical calculation of the signal-to-noise ratio (SNR) in a 20 nm  $\times$  20 nm SOT reader with CoFe (3 nm)/MgO (0.8 nm)/BiSb (5 nm) stack, and found that the required minimum  $\theta_{SH}$  was about 2 at the bias current is 400  $\mu$ A to achieve SNR  $\geq$  28 dB.

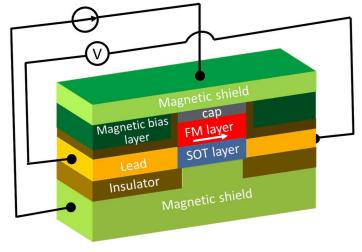


Figure 5. Schematic illustration of a SOT reader as viewed from a media facing surface.

We then demonstrated proof-of-concept of BiSb-based SOT readers. Here, we used top BiSb/MgO/CoFe for higher spin Hall angle. The fabrication of SOT reader consists of six cycles of optical lithography, magnetron sputtering deposition, and lift-off process. Figure 6(a) shows the schematic device structure. First, we prepared a Ta (15 nm) / Pt (5 nm) bottom electrode (I-) on an oxidized silicon substrate. Then, we deposited a pillar of CoFe (5 nm)/MgO (2 nm)/BiSb (10 nm)/Pt (1 nm) with the size of 20  $\mu$ m × 20  $\mu$ m. The Pt layer works as a capping layer to prevent possible damage to the BiSb layer from wet process and air exposure. In this demonstration, we chose CoFe because of its high spin polarization. The interfacial layer of MgO is used to further enhance the spin polarization thanks to the spin-filtering effect [42,43,44] and prevent damage of the CoFe layer due to Sb diffusion during BiSb sputtering. Next, we deposited an insulating layer and two side electrodes (V- and V-). After that, we deposited another insulating layer to create a window for current injection. Finally, we deposited a top electrode (I-) of Ta (45 nm) / Pt (15 nm) on top of the pillar. Figure 6(b) shows a top-view optical image of a completed device and the experimental setup. We applied a perpendicular bias charge current to the pillar via the current injection window (8  $\mu$ m× 20  $\mu$ m), and measured the output voltage V<sub>ISH</sub> between the two side electrodes (V- and V-) while sweeping an in-plane external magnetic field H<sub>x</sub> along the x direction.

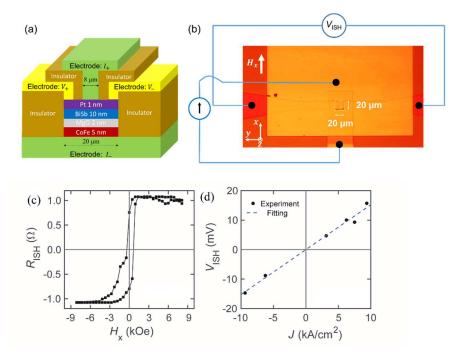


Figure 6. Schematic illustration of a SOT reader as viewed from a media facing surface.

Figure 6(c) shows the  $R_{\rm ISH}$  resistance curve, defined as  $R_{\rm ISH} = V_{\rm ISH}/I$ , of a device measured with a bias current density  $J = 6.3 \text{ kA/cm}^2$  at room temperature. The  $R_{\rm ISH}$  is as large as 1.1  $\Omega$ . Figure 6(d) shows the  $V_{\rm ISH} - J$  characteristics of this device.  $V_{\rm ISH}$  reaches 15 mV at  $J = 9.4 \text{ kA/cm}^2$ . We estimate a giant  $\theta_{\rm SH} = 61$  in this device. This value is close to  $\theta_{\rm SH} = 52$  originally observed in epitaxial top BiSb/MnGa grown by molecular beam epitaxy [4], where the BiSb has the pseudo-cubic (012) orientation. This large  $\theta_{\rm SH}$  will allow a very low bias current of only 13.5  $\mu$ A or  $3.38 \times 10^6 \text{ A/cm}^2$  in 20 nm  $\times$  20 nm SOT reader, and reserve a large margin for further device scaling beyond 4 Tb/in². Our results showcase the potential of BiSb for SOT reader beyond 4 Tb/in² magnetic recording technology. Last but not least, the results in this work can also be applied to the output stage in magnetoelectric spin—orbit (MESO) logic devices, recently proposed as an alternative to Si transistors for very low power consumption [45].

We also demonstrated an alternative setup for the SOT sensor, in which the direct spin Hall (DSH) effect, rather the inverse spin Hall (ISH) effect, was used for sensing [11]. Figure 7(a) shows the schematic illustration of the multilayer stacking used in this work, with a bottom BiSb layer /interlayer/CoFe FM layer, deposited at Western Digital facility. Figure 7(b) shows the direct spin Hall sensor device structure and the measurement setup. Figure 7(c) shows an optical image of a fabricated device. Figure 8 shows a representative  $R_{\rm DSH}$  resistance curve, defined as  $R_{\rm DSH} = V_{\rm DSH}/I_{\rm DC}$ , measured with  $I_{\rm DC} = V_{\rm DSH}/I_{\rm DC}$ .

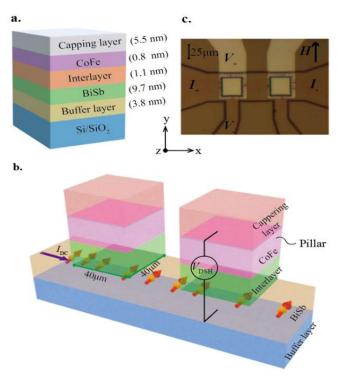


Figure 7. Schematic illustration of a SOT reader as viewed from a media facing surface.

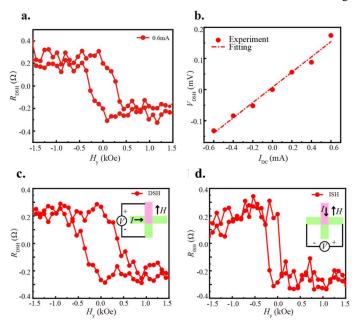


Figure 8.  $R_{\rm DSH}$  measured with a bias current  $I_{\rm DC} = 0.6$  mA at room temperature. (b) The relationship between the  $V_{\rm DSH}$  and the bias current  $I_{\rm DC}$ . (c)(d) Comparison between  $R_{\rm DSH}$  and  $R_{\rm ISH}$  at  $I_{\rm DC} = 0.2$  mA.

0.6 mA at room temperature while sweeping an in-plane magnetic field  $H_y$ . A large  $R_{\rm DSH}$  of 0.27  $\Omega$  is obtained, which is three orders of magnitude larger than the 0.14 m $\Omega$  expected for the anomalous Hall resistance with the in-plane  $H_y$ . Furthermore, we observed that the voltage  $V_{\rm DSH}$  is a linear function of  $I_{\rm DC}$  as shown in Fig. 8(b), which eliminates any thermomagnetic effects, such as the anomalous Nernst effect, as the origin of the observed signal. Figures 8(c) and 8(d) compare  $R_{\rm DSH}$  and the  $R_{\rm ISH}$ =  $V_{\rm ISH}/I_{\rm DC}$  obtained with a perpendicular  $I_{\rm DC}$  injected into the pillar from the top electrode and

the voltage  $V_{\rm ISH}$  generated in the BiSb layer. Here, both data were obtained with the same  $I_{\rm DC}=0.2$  mA. One can see that both the data yield the same output magnitude, thus confirming the reciprocal between the DSH and ISH in our device. Note that the observed  $R_{\rm DSH} \sim R_{\rm ISH} \sim 0.27~\Omega$  in our 40 µm-wide pillar is comparable to  $R_{\rm ISH}=0.1~\sim1~\Omega$  observed in our 20 µm-wide ISH sensing device comprised of CoFe 5 nm/MgO 2 nm/ top BiSb 10 nm. We estimate a colossal  $\theta_{\rm SH} \sim 164$  in this device. However, the noises in this device are significantly higher than in the previous work, which is due to the dominant spin-transfer noise. Nevertheless, the observed  $R_{\rm DSH}$  or  $R_{\rm ISH}$  in our devices are significantly larger than  $R_{\rm ISH}$  observed in Ta/MgO/CoFeB or Pt/MgO/CoFe devices [46], confirming the advantage of using BiSb for SOT sensor application. We note that unlike SOT-MRAM, the SOT sensor requires only 230°C thermal budget for manufacturing. Thus BiSb-based SOT sensor is feasible for the first realistic device application of topological insulator.

#### 5. CONCLUSION

BiSb is the only topological insulator that satisfies the three conditions for SOT device manufacturing: (1) a large spin Hall angle of the order of 10, (2) large electrical conductivity  $\sigma$  of order of  $10^5 \Omega^{-1} \text{ m}^{-1}$ , and (3) can be deposited using sputtering deposition. In the past 5 years, we have collaborated with major memory device vendors to explore the potential of BiSb for applications to SOT-MRAM and SOT sensor. Our works showcase the feasibility of topological materials with the giant spin Hall effect for device applications.

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