Ph. D. Dissertation

Integration of BiSb topological insulator and ferromagnetic multilayers for magnetic storage devices

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Abstract

Topological insulators (TIs) are quantum materials with a strong spin Hall effect originating from the topologically protected surface states. With such attractive features, TIs have become candidates for many magnetic storage devices such as spin-orbit torque (SOT) magnetoresistive random access memories (MRAM), racetrack memories, spin Hall oscillators, and hard disk drive (HDD) readers. Among TIs, BiSb has stood out as a conductive TI with a colossal spin Hall effect. In this dissertation, we focus on integrating BiSb with ferromagnetic multilayers for magnetic storage devices. This work is structured as follows.

In Chapter 1, we quickly review the history of computer and memory development. We show how computing demand has sharpened the memory industry throughout history. This chapter ends by introducing the rising demand for ultralow power consumption, high speed of operation, and ultrahigh bit-density memory devices for the futuristic artificial intelligent computing.

In Chapter 2, we present the fundamental physics of spin-related phenomena in spin Hall materials. This chapter also delves into the properties and spin Hall effect of BiSb TI, which distinguishes them from other TIs and conventional heavy metals.

In Chapter 3, we introduce the fabrication tools and the characterization techniques used in this dissertation.

In Chapter 4, we demonstrate a proof-of-concept SOT reader using the large inverse spin Hall effect of BiSb. Starting with a noise analysis of the reader, we identify that BiSb must have a spin Hall angle of larger than 2 to achieve a sufficient signal-to-noise ratio of 28 dB using a bias current of 400 μA. Afterwards, we perform the spin Hall angle optimization by integrating BiSb together with typical ferromagnetic materials such as Co, CoFeB, NiFe, and CoFe. A large spin Hall angle of 5.1 was observed in the stack of BiSb/MgO/CoFe/Buffer on Si/SiO_x substrate. Finally, we adopted and modified this stack to fabricate the SOT reader. Our SOT reader shows a giant inverse spin Hall angle of 61 that is capable of generating a large output voltage of 15 mV with 9.4 kA/cm^2. This performance is approximately two million times stronger than that of the Pt-based SOT reader, which indicates the potential

of BiSb for use in the SOT reader for beyond 4 Tb/in^2 HDD technology.

In Chapter 5, we develop a perpendicular magnetized anisotropy (PMA) CoFeB/MgO and bottom BiSb stacks using an oxide interfacial layer for ultralow power SOT-MRAM cache memory. By integrating CrO_x (chromium oxide) as the interface between BiSb and CoFeB/MgO, we can realize the PMA and obtain a relatively large spin Hall angle of 2.8. The dependence of the spin Hall angle on the CrO_x thickness can be explained by the extrinsic factor, i.e., spin transparency of CrO_x, and the intrinsic factor, i.e., the suppression of Sb migration by the CrO_x barrier. Eventually, we achieve the SOT magnetization switching by a small current density of 3.1 MA/cm^2 with a pulse width of 50 µs, which is an order of magnitude smaller than that in heavy metals. Via the thermal activation model, we estimate a bit retention of more than 500 seconds, which could be sufficient for last-level SOT-MRAM cache memory applications.

In Chapter 6, we address concern about the manufacturability of BiSb. Although BiSb has displayed an appealing performance, the low melting point of approximately 280°C quickly drives the interests away due to the incompatibility with the back-end-of-line manufacturing process. To overcome this obstacle, we introduce a melting and recrystallization process of BiSb at 400°C that not only satisfies the thermal budget requirement but also preserves the PMA and the large spin Hall angle as well as induces single-phase BiSb. It is worth noticing that the single-phase BiSb, so far, has been realized only on the crystallized substrates such as GaAs, c-plane sapphire, and BaF_2. Such a process is facilitated by sandwiching BiSb between oxide buffer/seed layers and a protection layer. The maximum spin Hall angle of 7.6 and a small threshold switching current density of 1.3 MA/cm^2 at 50 µs were observed in the melted and recrystallized samples. This result indicates the potential of integrating BiSb with CMOS electronics for the mass production of BiSb-based SOT-MRAM and other magnetic memory applications.

Finally, Chapter 7 concludes the dissertation.

List of Abbreviations (in chronological order)

Abbreviation	Description
CPU	center processing unit
LLC	last-level cache
RAM	random access memory
SRAM	static random access memory
DRAM	dynamic random access memory
CMOS	Complementary Metal-Oxide-Semiconductor
WL	wordline
BL	bitline
AI	artificial intelligence
HDD	hard disk drive
SSD	solid state drive
GMR	giant magnetoresistance
NM	non-magnetic
FM	ferromagnetic
CPP	current-perpendicular-to-plane
TMR	tunnel magnetoresistance
MTJ	magnetic tunnel junction
MRAM	magnetoresistive random access memory
AFM	anti-ferromagnetic
STT	spin transfer torque
SNR	signal-to-noise ratio
SOT	spin orbit torque
SHE	spin Hall effect
ISHE	Inverse spin Hall effect
SHA	spin Hall angle

SEM	scanning electron microscopy
HM	heavy metal
SOC	spin-orbit coupling
SOI	spin-orbit interaction
TI	topological insulator
REE	Rashba-Edelstein effect
AHE	anomalous Hall effect
PMA	perpendicular magnetic anisotropy
TSS	topological surface state
TRS	time-reversal symmetry
MBE	molecular beam epitaxy
BEOL	back-end-of-line
RP	rotary pump
TMP	turbo-molecular pump
GV	gate valve
DC	direct current
RF	radio frequency
XRD	X-ray diffraction
XRR	X-ray reflectivity
SQUID	superconducting quantum interference device
TEM	transmission electron microscopy
IMA	in-plane magnetic anisotropy
AC	alternating current
ONE	ordinary Nernst effect
ANE	anomalous Nernst effect
SSE	spin Seebeck effect
p-MTJ	perpendicular magnetic anisotropy magnetic tunnel juntion
FWHM	full width at half maximum

List of Symbol

Symbol	Description
$\hbar$	reduced Planck constant
k_{B}	Boltzmann constant
μ_{B}	Bohr magneton
g	Landé g factor
e	electron charge
μ_0	the vacuum permittivity
α	damping constant
γ	gyromagnetic constant
v_{F}	Fermi velocity
$\vec{\sigma}$	spin polarity vector
P	spin polarization
M_{s}	saturation magnetization
V_{X}	volume of X layer
w_{X}	width for X layer
t_{X}	thickness for X layer
J_{X}	charge current density for X layer
ρ_{X}	resistivity for X layer
σ_{X}	conductivity for X layer
$R_{\mathrm{sheet}}^{\mathrm{BiSb}}$	BiSb sheet resistance
$t_{\mathrm{surface}}^{\mathrm{BiSb}}$	BiSb surface state thickness
$J_{\mathrm{th}}^{\mathrm{BiSb}}$	threshold current density for BiSb layer
$\sigma_{\mathrm{bulk}}^{\mathrm{BiSb}}$	bulk states conductivity of BiSb
$\sigma_{\mathrm{surface}}^{\mathrm{BiSb}}$	surface states conductivity of BiSb
J_0^{BiSb}	threshold current density for BiSb layer at 0 K
E_{g}	band gap

Δ	thermal stability factor
$1/\tau_0$	attempt switching frequency
$\tau_{\mathrm{retention}}$	bit retention
f	bandwidth
T	temperature
λ_{sf}	spin diffusion length
H_{stiff}	the bias field from the magnetic bias layer
c	the amplifier noise constant
θ_{SH}	spin Hall angle
σ_{SH}	spin Hall conductivity
R_{H}^{ω}	first harmonic Hall resistance
$R_{\mathrm{H}}^{2\omega}$	second harmonic Hall resistance
V_{H}^{ω}	first harmonic Hall voltage
$V_{\mathrm{H}}^{2\omega}$	second harmonic Hall voltage
R_{ISH}	inverse spin Hall resistance
V_{ISH}	inverse spin Hall voltage
R_{AHE}	anomalous Hall resistance
$R_{\mathrm{ANE+SSE}}$	ANE/SSE resistance
R_{ONE}	ONE resistance
H_{z}	out-of-plane external magnetic field
H_{x}	in-plane external magnetic field
H_{k}	effective magnetic anisotropy field
H_{AD}	damping-like SOT effective field
I	bias current
I_{s}	spin current
J	bias current density
J_{s}	spin current density

Contents

Chapter 1: Introduction to magnetic storage devices

The ongoing evolution and development of technology has shaped our society in ways we could have never imagined. It has transformed the manner in which we interact, engage in work, and conduct our everyday lives. Understanding the modern technological world involves a comprehension of its historical context. Nowadays, computers are indispensable in our modern lives. When discussing a computer, it is impossible not to mention its memories. To perform the tasks, from the easiest to the most complicated, memories supply information and store the computing results. In this chapter, we will cover a brief introduction of computer and memory development, starting from the dawn of computer to the forecast of memory technologies for advanced computing applications.

1.1 Mechanical computer

1.1.1 The dawn of computer

Long before the emergence of modern computers, people had attempted to realize a system that could solve complex problems without human error. The initial efforts to construct such systems were mainly based on the integration of mechanical components, including gears, wheels, and levers, for data representation and manipulation. Discovered in a shipwreck along the Greek coast, the 2nd-century BCE Antikythera mechanism is believed to be the oldest mechanical computer of the human civilization [1]. This device employs a complex system of bronze gears to calculate the movements of celestial bodies and forecast astronomical phenomena such as eclipses. Each gear's rotations represent the necessary data for precise

calculations. When the gears align, they display a unique astronomical cycle. In essence, the Antikythera mechanism illustrates the results of astronomical calculations through the mechanical movements of the gears. This device indicates that people were trying to automate the representation of information long before electronic computers.

Since then, automation was gradually introduced into daily life. The Islamic golden age inventor Al-Jazari, who is recognized as the father of robotics, created several systems that used gears and spinning parts to conduct programming-like motions, mimicking human gestures. His famous inventions include water supply systems and clocks. However, there was no progress toward a computer capable of performing arithmetic calculations. Until the Renaissance period, Leonardo da Vinci conceptualized a mechanical calculator that utilized gears for arithmetic operations – a concept that culminated in the Pascaline 150 years later. Unfortunately, he never built them. Even so, da Vinci's designs reveal a growing interest in using mechanical systems to represent and process data in a structured, programmable way.

1.1.2 Arithmetic capabilities

By the 17th century, inventors had begun to create machines specifically designed to perform arithmetic operations with mechanical components. Blaise Pascal invented the Pascaline in 1642, making it one of the leading devices at the time. This mechanical calculator employed geared wheels to add and subtract integers, which shares some commons with Da Vinci's sketches. Each wheel represented a number, and as it rotated, it would transmit the values to the next wheel until it reached ten, imitating how humans do arithmetic.

In the late 17th century, Gottfried Wilhelm Leibniz invented the Stepped Reckoner, a successor of the Pascaline. The Stepped Reckoner further completed the Pascaline by featuring multiplying and dividing functions. A new stepped drum mechanism allowed repeated additions and subtractions, which constitutes multiplication and division. The gear configurations and their interactions expressed the numbers and calculations under operation. On top of this contribution, Leibniz was obsessed by the idea of expressing the universe in the simplest form. Inspired by the ancient Chinese Yi ching of broken and solid lines, Leibniz

digitalized them into "0" and "1" through the concept of binary representation. This later became the founding stone for electronic computing and memory.

Perhaps Charles Babbage's Difference Engine and later his Analytical Engine marked the peak of mechanical computers. The complex mechanical design of the Difference Engine allowed it to tabulate polynomial functions, while the Analytical Engine was considered the climax of a mechanical computer with mass storage and programmability. "The store," a mechanical memory module, could hold up to 1,000 figures, each with 50 digits, serving as a record of that time [2]. Additionally, it utilized punched cards to program "the mill," a module similar to that of a central processing unit (CPU). Then, this mill could retrieve data from the store and perform pre-programmed calculations. This design was considered the first to enable efficient data accessibility. However, due to the rapid growth of societies, the computing demand quickly outpaced the capabilities of mechanical computers.

1.1.3 Electro-mechanical computer

The emergence of electrical engineering and the demand to solve complex mathematic problems fueled the transition from purely mechanical systems to electro-mechanical computers in the beginning of the 20th century. This innovative wave combined electrical components with mechanical parts for data encoding and processing. For example, Konrad Zuse's Z3 (1941) represented data with relays and switches that could toggle between positions to indicate binary states. In 1944, the IBM Harvard Mark I employed a combination of electrical relays and mechanical components, including rotating wheels, for data storage and analysis. These components encoded data, enabling the machine to perform arithmetic operations autonomously. With the integration of electrical modules, these electro-mechanical computers made a significant advancement toward modern computers.

1.1.4 Electronic computer

The ENIAC (Electronic Numerical Integrator and Computer), built in 1945, was the first entirely electronic, general-purpose computer, representing a significant advancement

in computing technology. Unlike its predecessors, the ENIAC used vacuum tubes to do computations electronically, allowing it to run at unparalleled speed up to 5,000 additions per second. However, to reprogram the ENIAC, operators had to manually wire its circuits, which did not provide a user-friendly interface.

Behind the success of the ENIAC, there was a significant contribution from Von Neumann. He later proposed a computer architecture with stored program memory, which allowed for the storage of instructions. This invention, which highlighted the importance of memories storing both data and instructions, had opened a new area for computing.

To summarize the early development of computers, we show a timeline of pre-Von Neumann computer evolution in Figure 1.1.

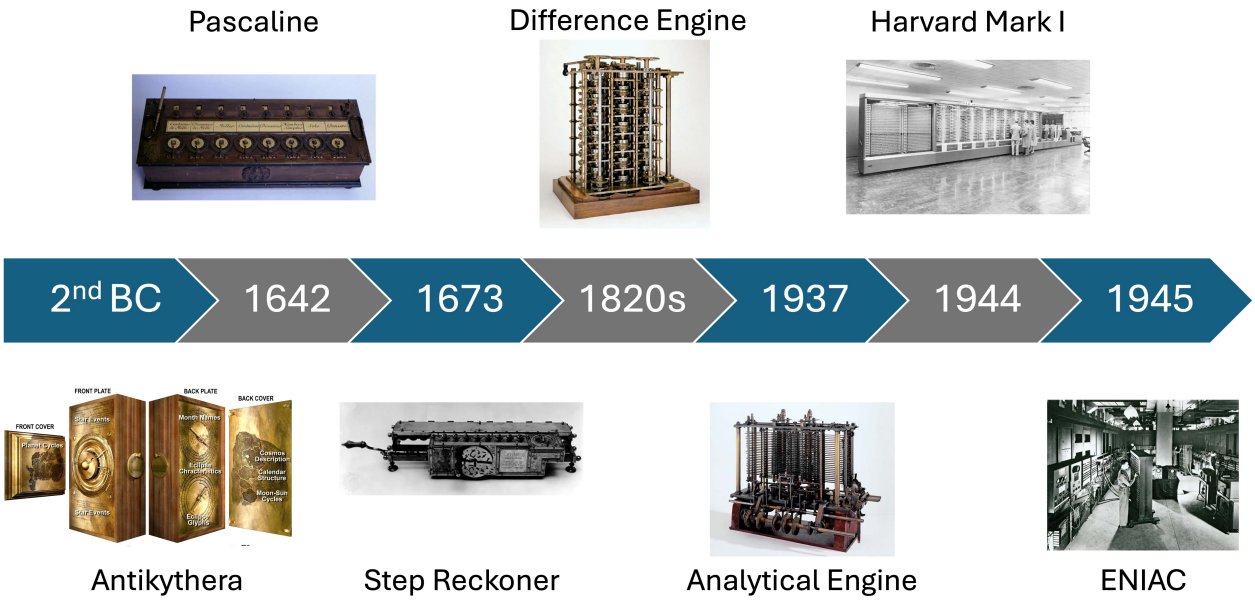

Figure 1.1: Timeline of computer evolution before Von Neumann architecture. Images reproduced with permission of the rights holders, Springer Nature and Britannica.

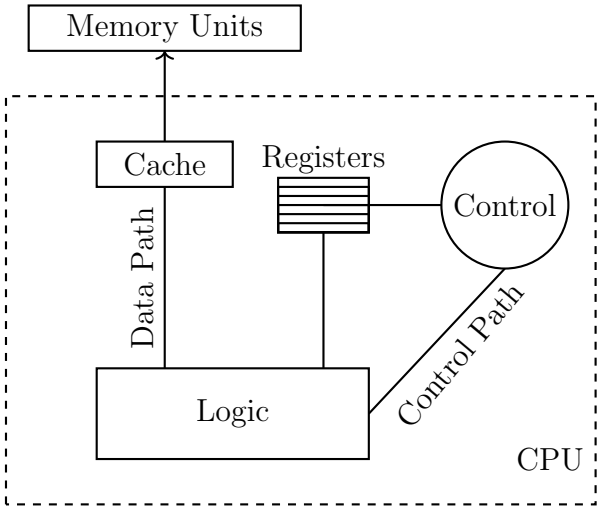

Figure 1.2: A schematic picture of Von Neumann architecture.

1.2 Memories in Von Neumann architecture

Von Neumann architecture has been widely in use in computers since 1945. His idea can be simplified as a CPU interconnected with other memory units [3]. Figure 1.2 shows a schematic picture of the architecture. Inside the CPU, there is a control unit to execute instructions, a logic unit to perform arithmetic calculations, register memories, and caches. The memory units, which account for a large portion of the architecture, can store both data and instructions. The memories are hierarchized into various levels depending on the capacity and speed as shown in Figure 1.3. The base corresponds to the largest storage size and slowest speed while the top is the fastest memory with limited capacity. In the following sections, we introduce the memories from the top to the bottom of the hierarchy.

1.2.1 Register memory

Register memories are located inside the CPU. The control unit can access both instructions and the corresponding datapaths stored in these registers. A special register called the program counter contains the next instruction to be executed by the control unit [4]. To meet such a unique requirement, register memories have a limited capacity of 32 or 64 bits

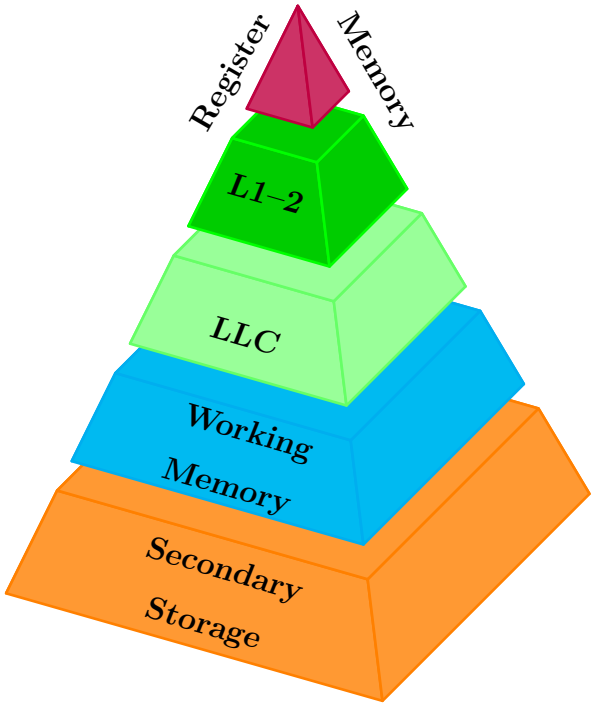

Figure 1.3: Memory hierarchy in Von Neumann architecture.

with extremely short bit retention and a latency of approximately a CPU cycle [5, 6].

1.2.2 Cache memory

Since the register memory is subjected to small capacity, the CPU needs additional storage nearby with a larger room but still guarantees relatively fast speed. Cache memory was designed to serve this purpose with two main functions. First, it keeps up with the CPU as it fetches and executes instructions. Second, it locates the information stored in the cache line, which loads the data from the slower memories [7].

Thus, cache memory is usually classified into three levels: on-chip L1, L2, and off-chip lower-level caches (LLC) (L3 – L4). The lower the level, the slower the speed, and the larger the capacity. Large caches likely hold data of interest, which lowers miss rates, but they are rather slower than small caches. The mechanism of fetching data from cache memories takes analogy as a water fountain, which shortens the average fetching time [8]. First, fetching instruction searches for the data in L1. When L1 cache misses, it moves on to check in

L2. The checking process continues on L3 and even main memory until the desired data is located. The Table 1.1 below summarizes the characteristics of different types of cache memories.

	L1	**L2**	**LLC**
Speed [8]	1 to 2 CPU cycles	Few tens CPU cycles	Hundred CPU cycles
Size [9]	8 kB to 1 MB	516 KB to 2 MB or greater	Few tens MB or greater
Location	Embedded on chip		Off chip

Table 1.1: A comparison between L1, L2 cache and LLC in terms of size, speed and location.

1.2.3 Working memory

Once the CPU exhausts the speedy cache memories, it sequentially relies on working memory for storing in-use data and programs. Despite being located off-chip, working memory is still sufficiently quick to enable relatively low-latency access to a larger pool of data. Data location can be randomly accessed within approximately equal access times, coining the term "random access memory (RAM)." Unlike cache, which has a limited capacity, working memory provides more storage space, enabling the system to run multiple processes concurrently. The flexibility of working memory makes it a crucial intermediary in the memory hierarchy, neutralizing the demand for both speed and volume in modern computing. The typical size of working memory can range from a few hundred MB to a few tens of GB.

1.2.4 Secondary memory

The memories mentioned above can be classified as short-term memories. Beyond that boundary, computers rely on secondary storage for the long-term retention of data. The prominent feature of long-term memory lies in its non-volatility, ensuring that data is preserved even in a blackout. While secondary storage is much slower than cache and working memory, it provides massive storage capacity over hundreds of GB, allowing users to store vast

amounts of data like files, applications, and system backups. Typically, secondary storage is accessed only when data needs to be loaded into working memory. Furthermore, scalability is one characteristic of secondary storage in the form of terminal memories. This allows users to expand the storage capacity by adding external memories. Compared to working memory or cache, secondary storage serves as a slower but essential module, guaranteeing the availability of data for future use. Hence, secondary storage serves as the last layer in the memory hierarchy, which sacrifices speed for volume and permanence.

In summary, Von Neumann architecture allows the CPU to execute instructions and access data stored in memories. This is achieved through a vast network of interconnections known as buses. Unfortunately, this design encountered a major problem when the amount of transmitted data increased dramatically. First, the high demand for data transmission between the CPU and memory consumes a significant amount of electrical energy. Second, due to size limitations of embedded memories, a part of in-use data is stored in a slower off-chip working memory. As a result, the working memory takes longer to deliver, which in turn slows down the overall processing speed. This problem is known as the memory bottleneck, which is a challenge for the realization of high-performance systems.

1.3 Present memory technologies

In this section, we introduce the present memory technologies for each component of the hierarchy.

1.3.1 Short-term memories

In the memory hierarchy shown in Figure 1.3, short-term memory commonly represents the top half. In this part, we will introduce static RAM (SRAM) and dynamic RAM (DRAM), which are the popular technologies for cache and working memories, respectively.

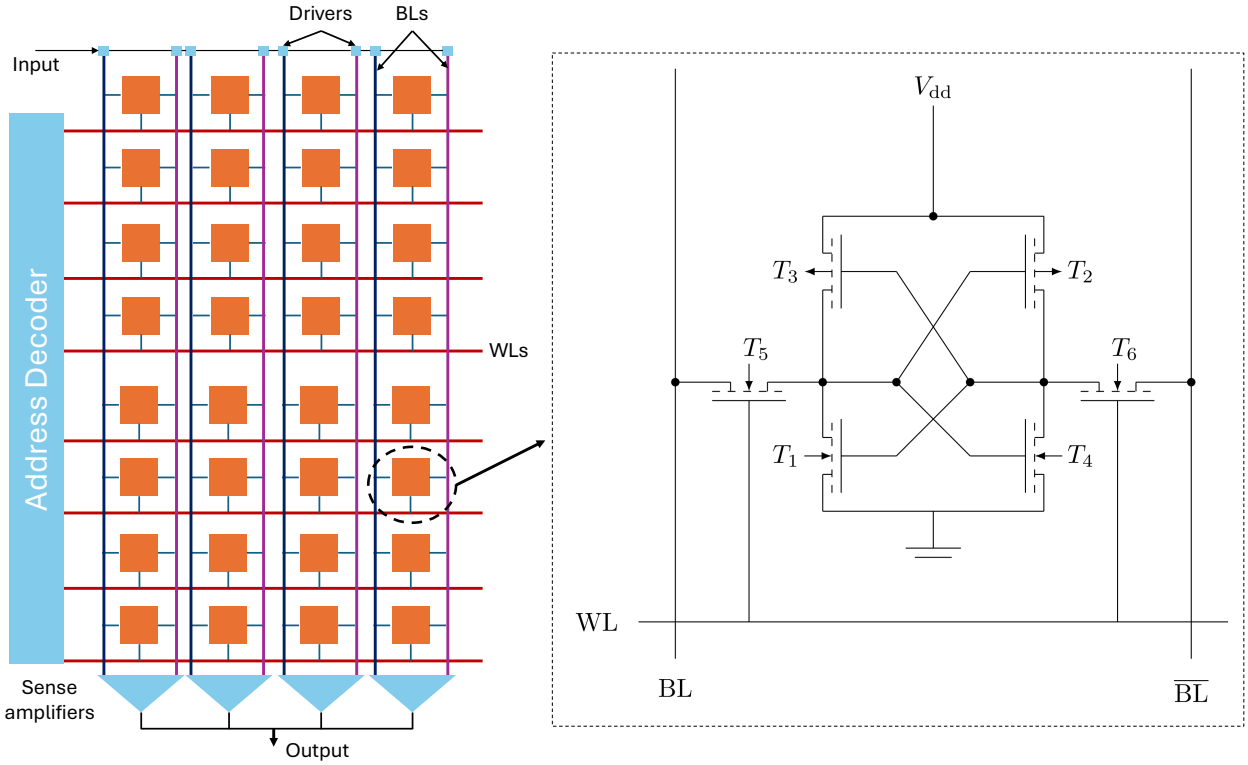

Figure 1.4: A schematic of a 8x4 SRAM array and the detailed schematic of a 6T-SRAM cell.

1.3.1.1 Static random access memory

SRAM is widely used in cache memories that require fast and reliable performance. An SRAM commonly uses six transistors to store a single bit of data: two as access gates (T_5, T_6) that control read and write access and four as a pair of cross-coupled complementary metal-oxide semiconductor (CMOS) inverters (T_1–T_4) [10]. Figure 1.4 displays the schematic of an SRAM array (left) and a detailed schematic of a 6T-SRAM cell (right). These two inverters create a bistable circuit, representing the binary system. To access the CMOS inverters for read and write, the wordline (WL) is set as high to open T_5 and T_6 gates and to connect them to the bitline (BL) and $\overline{\text{BL}}$. During idle times, the WL is set as low to close the T_5 and T_6 gates, thereby isolating the cell and preserving the data.

To read the data from an SRAM, first, BL and $\overline{\text{BL}}$ are pre-charged to V_{dd} and leave them

floating. Afterwards, the decoder sets a specific WL high to open T_5 and T_6 gates, connecting SRAM cells to BLs. Depending on the stored data, each cell in the activated WL gradually discharges one of the BLs to the ground. Eventually, the differential voltage between BL and $\overline{\text{BL}}$ is detected by a sense amplifier, which amplifies the difference and determines whether a '1' or '0' is stored.

To write the data, the drivers firstly set the BLs to desirable configurations, to express the "0" or "1" state. Secondly, the decoder sets a specific WL high to open T_5 and T_6 gates, connecting SRAM to the preconfigured BLs. With more power than CMOS inverters, the BLs overwrite the current state of the cell, flipping the bistable circuit to reflect the write data. Finally, the decoder deactivates WL, leaving the data secured inside the cell [11].

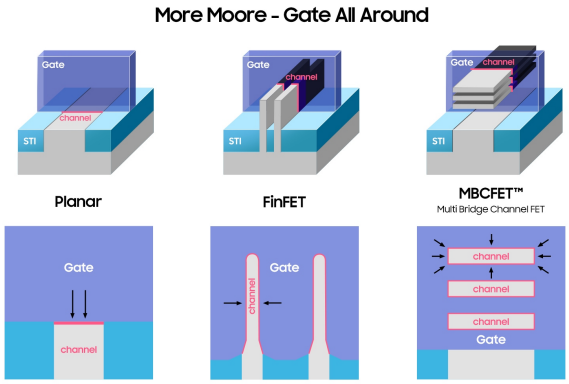

Figure 1.5: An illustration of Samsung 3 nm SRAM technology compared with previous technologies [12]. Copyright © Samsung.

After years of development, SRAM has achieved a latency of only a few tens of picoseconds and a power consumption of only a few nanowatts [13]. Fueled by the recent artificial intelligence (AI) chip race emphasizing the importance of energy efficiency, Samsung Foundry announced their advanced SRAM with Gate-All-Around technology providing a 22% speed and 34% power gain compared to the previous FinFET as shown in Figure 1.5 [14].

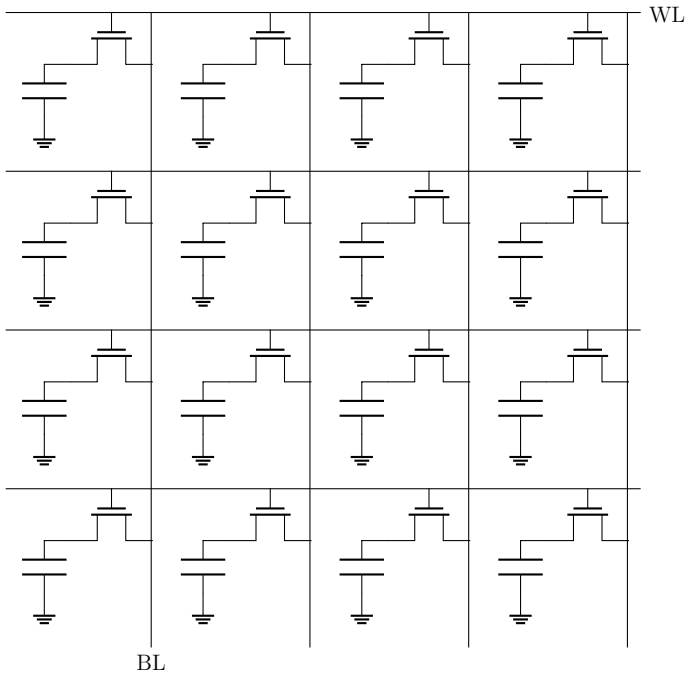

Figure 1.6: A schematic structure of a 4x4 array of 1T-DRAM cells.

1.3.1.2 Dynamic random access memory

To construct an SRAM cell, one need to fabricate many transistors, leading to a relatively low bit density and high cost of manufacturing. Stepping down from the hierarchy, DRAM uses fewer transistors per cell than the SRAM, which is favorable in terms of bit density. In general, DRAM comprises a gate transistor and a capacitor to store the data as charge as shown in Figure 1.6. Unlike SRAM, DRAM requires a refresh to preserve the data since the capacitors naturally discharge over time.

To read the data, first BL is precharged to an arbitrary value, i.e., $V_{\mathrm{dd}}/2$, before the decoder sets WL high, which connects the gate transistor to BL. The capacitor and BL share charges sequentially, causing a BL voltage drop when the capacitor discharges and a BL voltage rise when the capacitor charges. A sense amplifier then probes the voltage changes, determining "1" if the voltage exceeds a certain threshold and "0" otherwise. Unfortunately, the read operation in DRAM is destructive, in which all of the charges are released. Thus, after each read cycle, the data must be rewritten. This particular feature of DRAM signifi-

cantly reduces its energy efficiency down to 50% [15].

It is straightforward to write the data to a DRAM cell. Firstly, BL is precharged to V_{dd}, or ground, to represent the "1" or "0" state. The gate transistor connects to BL as soon as the decoder sets WL to high. Afterwards, the charge or discharge process takes place, storing either "1" or "0" in the capacitor. [11]

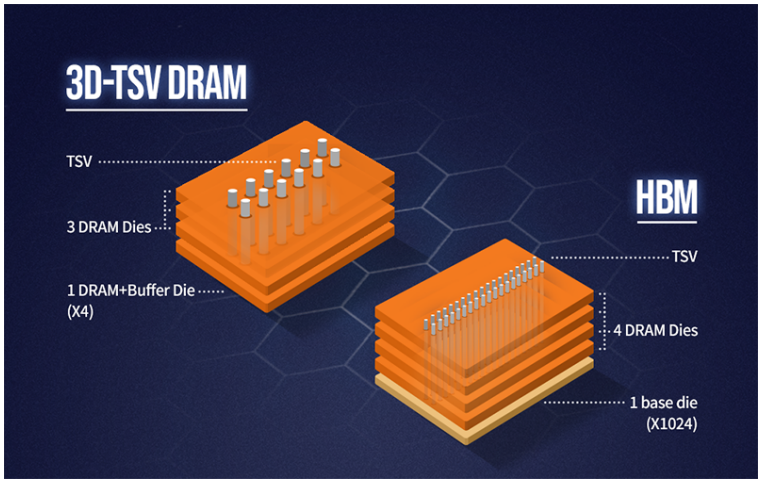

Figure 1.7: A schematic of 3D Through-Silicon-Via DRAM technology. Copyright © SK-Hynix.

Interestingly, advanced 3D stacking and the Through-Silicon Vias process can increase bit density by stacking DRAMs together. The schematic of this stacking structure is shown in Figure 1.7. During the AI race, the 3D DRAM has played a crucial role in the high-bandwidth memory. Recently, Samsung Foundry unveiled the HBM3 Icebolt chip, a DRAM-based chip with 12 layers of 10 nm-class 16 Gb DRAM dies, which offers 819 GB/s bandwidth for AI computing applications [16]. Additionally, proposals indicate that DRAM's energy consumption will reduce to approximately a few picojoules per bit [17].

In conclusion, for short-term memory, despite significant efforts by the semiconductor memory community to reduce power consumption, the inherent volatility of SRAM and DRAM requires standby energy to preserve data, even in an idling state. Indeed, this energy dissipation can account for up to 20% of the total energy consumption [18], which is an obstacle to ultralow-power and high-performance applications.

1.3.2 Long-term memories

Non-volatile technologies, which can preserve data for a substantial period, dominate the bottom half of the memory hierarchy in Figure 1.3. In this part, we will introduce NAND flash and hard disk drive (HDD), which are the current non-volatile storage technologies.

1.3.2.1 NAND flash

NAND flash memory is a non-volatile storage technology used in solid-state drives (SSDs), smartphones, USB drives, and memory cards. The use of NAND logic gates in its structure, which makes it highly efficient for storing large amounts of data in a compact form factor, gives it the name NAND.

A NAND cell simply consists of a floating-gate transistor where electrons can be stored for years. The read operation checks the cell's charge state, allowing the system to retrieve stored data. The write operation involves applying a higher voltage to place electrons on the floating gate, setting the cell to a specific state [19].

There are various types of NAND flash memory, including single-level cell (SLC), multi-level cell (MLC), triple-level cell (TLC), and quad-level cell (QLC). SLC NAND stores 1 bit per cell, making it the fastest and most durable but also the most expensive. MLC stores 2 bits per cell, while TLC stores 3 bits per cell, reducing cost but with lower durability and speed. QLC stores 4 bits per cell, maximizing storage density at the expense of performance and endurance.

Modern NAND flash focuses on enhancing storage density, speed, and durability through innovations such as 3D NAND, which features over 200 layers of stacking. These high-layer NAND chips are used in SSDs and high-capacity flash devices. SLC NAND can last over 100,000 program/erase cycles, while MLC, TLC, and QLC offer reduced endurance [20]. Nonetheless, this durability is insufficient for heavy read-write data processing in AI applications, which usually requires much higher program/erase cycles. A schematic structure of 3D NAND is shown in Figure 1.8.

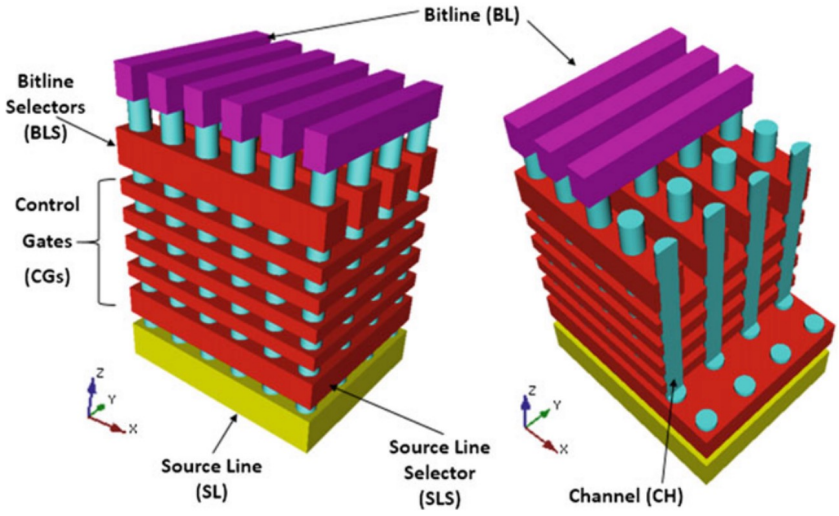

Figure 1.8: A schematic structure of 3D NAND [21]. Images reproduced with permission of the rights holders, Springer Nature.

1.3.2.2 Hard disk drive

HDDs, located at the bottom of the hierarchy, are famous for cost-effectiveness and large capacities. The main structure of an HDD consists of platters, a spindle motor, a read/write head, and an actuator arm as shown in Figure 1.9. HDDs store data magnetically on rotating platters coated with a magnetic material. The heads divide each platter into tracks and sectors to organize data. A spindle motor spins the platters at a constant speed, allowing data to be read and written by the heads. Read/write heads are tiny devices that hover above the platter surfaces on each side, reading data by sensing magnetic changes and writing by altering the magnetic direction. The actuator arm moves the read/write heads over the surface of the platters, controlled by a voice coil motor [22].

HDDs store data by magnetizing areas of the platter's surface in specific patterns. The write head creates a magnetic field that aligns the magnetic domains on the platter into two configurations, representing "0" and "1" states. The read head detects the magnetic orientation of each domain, interpreting it as binary data.

Recent demand from data centers has fueled the development of HDD-related technolo-

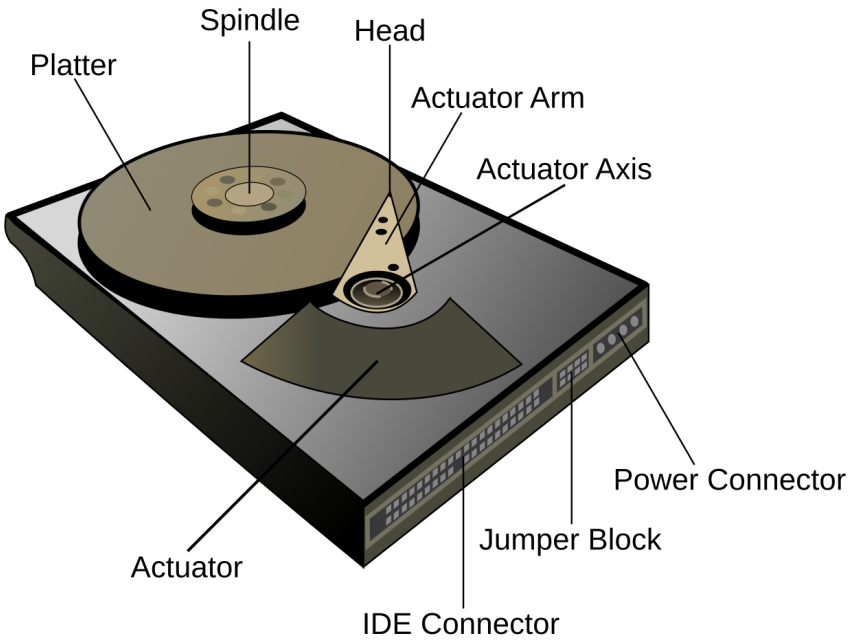

Figure 1.9: A schematic structure of a HDD. Source: Wikipedia - User: Surachit.

gies. Huge efforts have been dedicated to advance the areal bit density, including shingled magnetic and perpendicular magnetic recording to allow more data to be stored on a single platter [23]. Regarding the write head, heat-assisted magnetic recording and microwave-assisted magnetic recording technologies employ heat and microwave to enable higher data densities on the same surface area [24, 25]. To achieve completeness in HDD development, the read heads also need a big push. However, they continue to rely on sensors developed using early-stage spintronic technology, as we will discuss in the following section.

In summary, the current technologies in the memory hierarchy can be classified into two distinct groups: volatile memories (SRAM, DRAM) and non-volatile memories (NAND flash, HDD). The volatile memories at the top are fast, but they are subjected to high energy consumption, whereas the non-volatile memories at the bottom are subjected to relatively low speed. To reserve room for future demand, novel approaches are being explored as the alternatives for the current memory devices. Among the new technologies, spintronic devices are promising for ultralow power electronics and high bit-density magnetic storages.

1.4 Spintronic devices

Spintronics has emerged as an alternative to semiconductor technologies, offering solutions to the existing problems in the memory hierarchy. In this field, bits are demonstrated as spin directions, i.e., spin-up $\uparrow$ and spin-down $\downarrow$, rather than electron charge. In principle, spin is the intrinsic angular momentum of an electron. Noticeably, this quantity is preserved even in the absence of electrical power and can be manipulated by an external magnetic field. These features have enabled a distinct technology with low power consumption, non-volatility, and ultra-fast operation [26, 27, 28].

1.4.1 Giant magnetoresistance

The emergence of spintronics dates back to 1988, when A. Fert and P. Grünberg independently discovered the giant magnetoresistance (GMR) effect when examining the electrical resistance of Fe/Cr multilayers [29]. Generally, the GMR effect occurs in multilayer systems consisting of two or more ferromagnetic (FM) layers separated by a non-magnetic (NM) layer. This effect originates from spin-dependent scattering of conduction electrons at the interface of FM/NM multilayers and in the bulk of FM. On one hand, in the parallel state, electrons with spins aligned to the magnetization of the FM can easily pass through, lowering resistance to R_{P}. On the other hand, in the antiparallel state, electrons face increased scattering, especially for spins not aligned with the magnetization, which increases resistance to R_{AP}. Quantitatively, the GMR ratio characterizes this effect:

$$\text{GMR ratio} = \frac{R_{\mathrm{AP}} - R_{\mathrm{P}}}{R_{\mathrm{P}}}. \tag{1.1}$$

The current-perpendicular-to-plane (CPP) configuration can generate a higher GMR ratio [30]. An illustration of the GMR effect in the CPP mode is shown in Figure 1.10.

Regarding GMR applications, spin-valve devices have widely employed this effect for data storage and sensing technologies. However, the largest reported CPP-GMR ratio at room temperature in 2017 was only 73% [31], which is far behind the performance of another well-known spintronic effect, i.e., tunneling magnetoresistance (TMR).

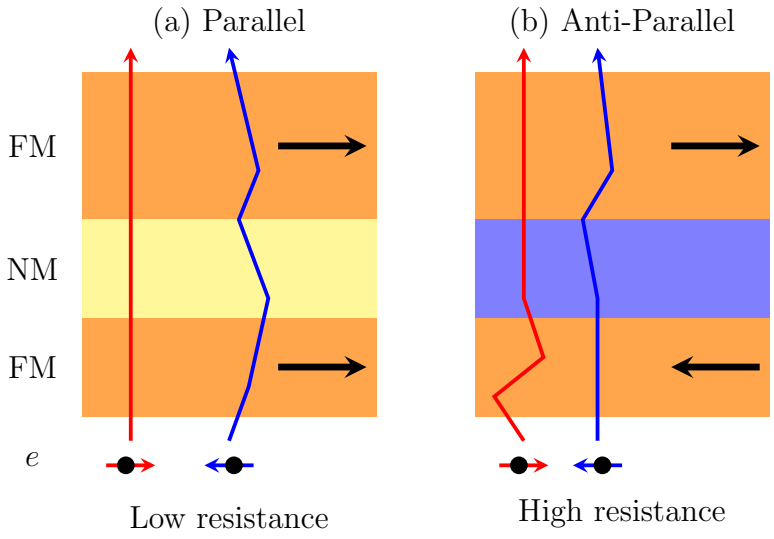

Figure 1.10: Schematic of the GMR effect when applying an out-of-plane current in (a) parallel configuration and (b) anti-parallel configuration.

1.4.2 Tunneling magnetoresistance

In 1975, M. Julliere observed the TMR effect in a heterostructure, where two FM layers sandwich an insulating material [33]. Such a junction is called a magnetic tunnel junction (MTJ). Unlike in the GMR effect, a spin-polarized current flows from one FM to the other owing to the quantum tunneling effect. This spin-polarized current is the combination of the currents for spin-up and spin-down electrons, each of them depending on the orientation of magnetization in the FM layers. The magnetization configuration between two FM layers determines the low or high resistance of the MTJ pillar, similar to the GMR effect. The spin-dependent tunneling occurs when spin-polarized electrons are transported through the barrier with the tunneling rate depending on the magnetization alignment of the FM layers as illustrated in Figure 1.11. Julliere's model determines the TMR ratio of an MTJ using the spin polarizations of the FM layers:

$$\text{TMR ratio} = \frac{2P_1P_2}{1 - P_1P_2}. \tag{1.2}$$

Here, P_1 and P_2 are the spin polarization of the FM layers, respectively. Unfortunately, a threshold of approximately 0.5 limits the spin polarization, which in turn restricts the TMR

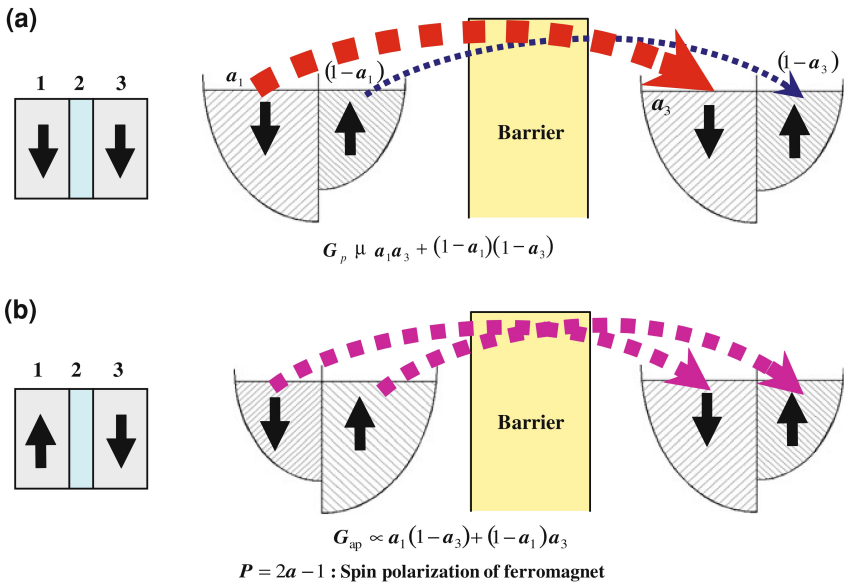

Figure 1.11: A illustration for spin-dependent tunneling mechanism of the TMR effect in parallel (a) and anti-parallel (b) configuration [32]. Images reproduced with permission of the rights holders, Springer Nature.

ratio. After numerous experiments to surpass the limitations of Julliere's model, a TMR ratio of up to 220% was found in the CoFe/MgO/CoFe junction in 2004 [34]. This was possible thanks to the spin-filtering effect of MgO [35, 36]. Until now, the largest room temperature TMR ratio reported in MTJs is 631% [37]. A summary of the development of TMR ratio until 2010 is shown in Figure 1.12 with a turning point at 2004. With impressive TMR ratios, spintronic devices such as HDD readers and magnetoresistive (MRAM) have employed the TMR effect to advance their performances.

1.4.2.1 HDD read head

Nowadays, TMR-based magnetic readers play a vital role in HDD technology [38]. Fundamentally, the structure of a TMR reader consists of an anti-ferromagnetic (AFM) layer to pin the fixed layer by coupling field, and an MTJ. Additionally, the free FM layer can extract the information from the magnetic recording medium through the change in its magnetization. The tunneling barrier separates the two FM layers, completing the MTJ structure.

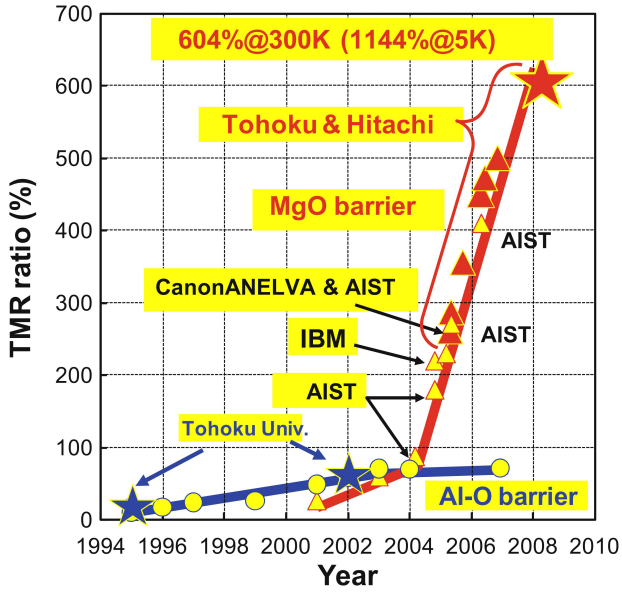

Figure 1.12: The development of TMR ratio until 2010 [32]. Image reproduced with permission of the rights holders, Springer Nature.

As a result of the TMR effect, the magnetoresistance in the reader is changed accordingly, depending on the parallel or anti-parallel state. A simple schematic of the TMR reader inside an HDD is shown in Figure 1.13.

As the HDD technology enters the phase beyond 4 Tb/in^2 [39], the TMR readers encounter several technical challenges in preserving a sufficient signal-to-noise ratio (SNR) and scalability. Unavoidably, the working principle of the TMR reader introduces an additional spin-transfer torque (STT) noise. On top of that, the thermal noise substantially increases as scaling down the size, which is an obstacle for achieving a good SNR at smaller dimensions [40]. Moreover, the complexity of a multilayer TMR reader prevents its shrinkage below 20 nm for higher bit density purpose. Hence, alternative technologies should be studied to attain the future of beyond 4 Tb/in^2 HDDs.

1.4.2.2 Magnetoresistive random access memory

MRAM is a non-volatile memory that stores data as the anti-parallel and parallel states of an MTJ, making it appealing in terms of speed and durability. In conventional MRAM,

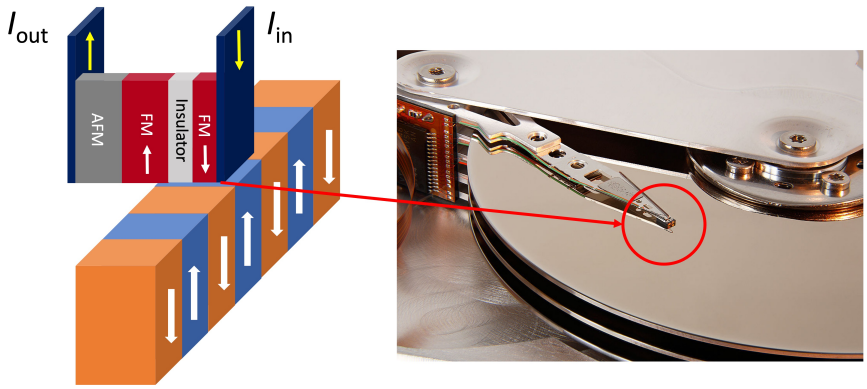

Figure 1.13: Schematic of the TMR reader inside an HDD. Sources: Wikipedia Commons - Eric Gaba.

the magnetization of the free layer is toggled using Oersted field created by electric currents, which is not favorable regarding writing energy. The schematic structure of this MRAM is shown in Figure 1.14 (a).

The successor, spin-transfer torque (STT)-MRAM, is an advanced version that uses spin-polarized currents instead of Oersted field to exert spin-transfer torque onto the magnetization, allowing for more energy-efficient and faster operation. The schematic structure of the STT-MRAM is shown in Figure 1.14 (b). Currently, various embedded and standalone STT-MRAM commercial products are available on the market, marking the maturity of these technologies [42, 43]. However, the challenges of STT-MRAM include gigahertz range operation, scalability, reliability and most importantly, STT efficiency. Due to the nature of STT, the writing current must be supplied for several nanoseconds to completely switch the magnetization, resulting in a significant delay for high-level cache applications [44]. The details mechanism will be discussed in Chapter 2. The STT efficiency can be expressed via the magnitude of spin-polarized current as follows:

$$I_{\mathrm{s}} = P\frac{\hbar}{2e}I_{\mathrm{c}}. \tag{1.3}$$

Given that the spin polarization is less than 1, a large charge current must be applied to create a substantial spin-polarized current to switch the magnetization via the STT effect [45]. Therefore, the STT-MRAM has not yet reached a full potential of ultrafast and low-

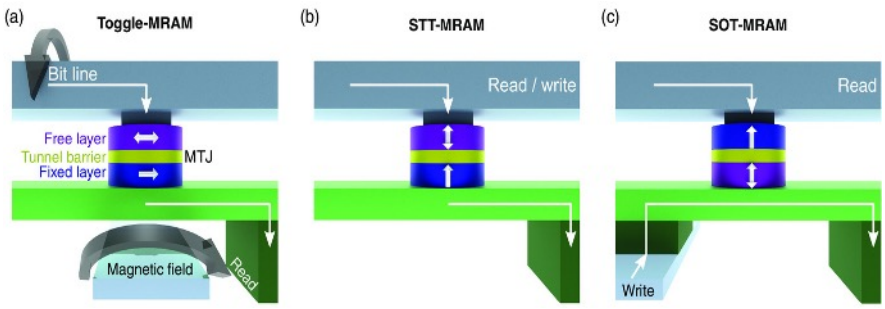

Figure 1.14: The evolution of MRAM: (a) The first generation of MRAM uses magnetic fields to flip the magnetization in an MTJ. (b) The second generation - STT-MRAM use spin-polarized current to write their cells. (c) Third generation - SOT-MRAM uses pure spin current from the SHE to write the data [41]. Image reproduced with permission of the rights holders, Willey.

power spintronic devices. The low STT efficiency also presents a challenge to scalability, as the size of the selecting transistor must be sufficiently large to support a large writing current [46]. Hence, further engineering efforts and novel technologies should be explored to replace SRAM with MRAM in the high-level caches. To conclude this section, we present the current memory hierarchy, which still relies mainly on the volatile semiconductor memories, as shown on the left of Figure 1.15. In the upcoming section, we will delve into recent technologies based on spin-orbit torque (SOT) effects that can define a new non-volatile memory hierarchy.

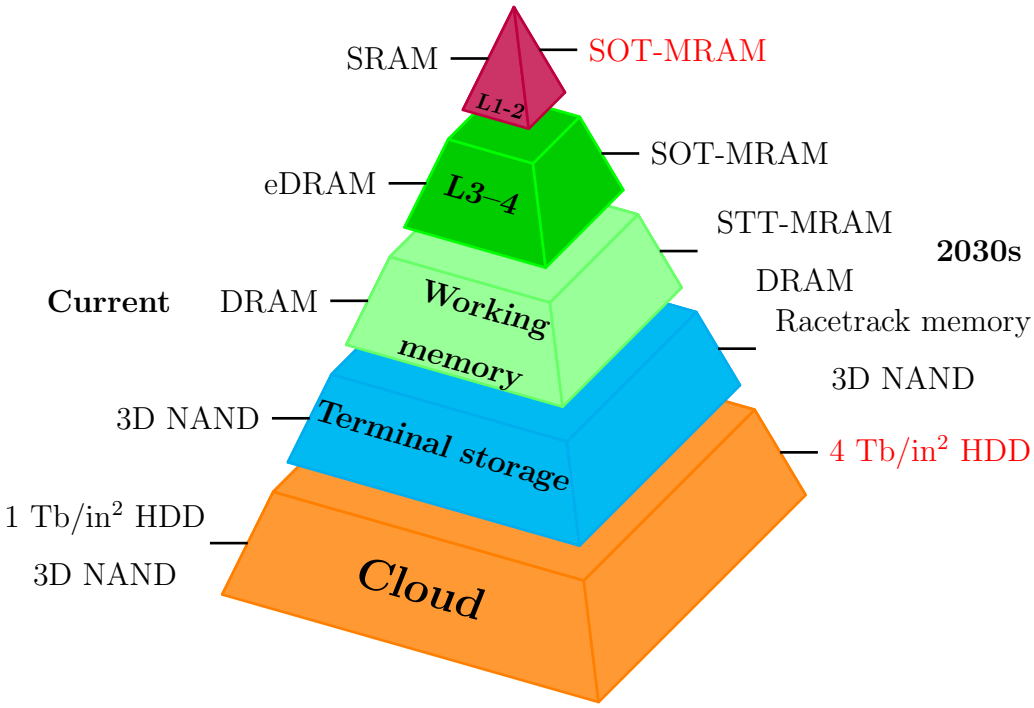

Figure 1.15: Memory hierarchy at the moment (left) and the vision in 2030s (right).

1.5 Spin-orbit torque magnetic storage device

1.5.1 Spin-orbit-torque reader

Recently, an SOT reader utilizing the inverse spin Hall effect (ISHE) was proposed with the potential of serving as a successor to the TMR reader [47]. An SOT reader is composed of an FM layer and a heavy metal (HM) layer, which serves as a spin Hall material, as illustrated in Figure 1.16. When a perpendicular spin-polarized current is injected from the FM layer into the HM layer, an in-plane charge current is generated as a result of the ISHE. The direction of magnetization determines the polarity of the output voltage, which is controlled by an external magnetic field. This SOT reader can provide three distinct advantages compared with the TMR reader. First, the simple structure of bilayer HM/FM enables scalability for high bit-density applications. Second, unlike the TMR reader, there is no additional STT noise. Most importantly, the thermal noise remains independent of the

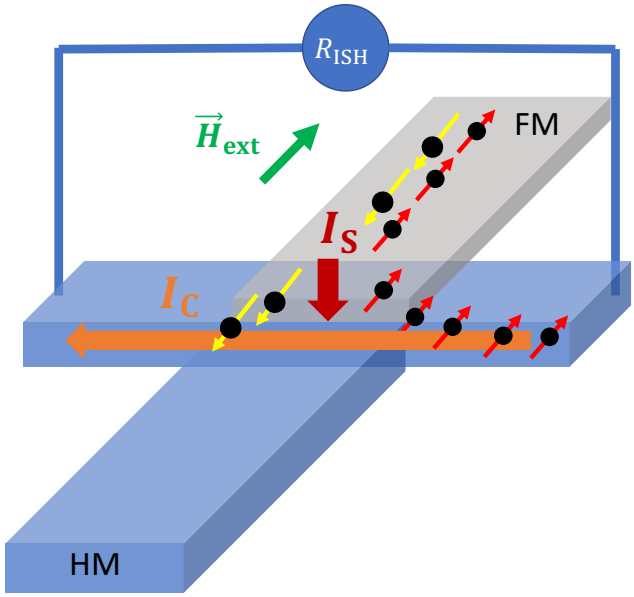

Figure 1.16: A schematic structure of the SOT reader consisting a FM layer and a HM layer.

spatial dimension, which allows scaling without degrading the SNR.

1.5.2 Spin-orbit torque Magnetoresistive random access memory

SOT-MRAM is a next-generation MRAM technology that is expected to fulfill the potential of ultrafast and ultralow-power consumption of MRAM technology. The SOT-MRAM consists of an MTJ, akin to the previous STT-MRAM, and a spin Hall layer, functioning as a spin current injector. When receiving an in-plane charge current, the spin Hall layer injects a perpendicular pure spin current to the free FM layer as a result of the spin Hall effect (SHE). Then, this pure spin current exerts spin-orbit torque, which can flip the magnetization to create the binary states. The schematic structure of the SOT-MRAM is shown in Figure 1.14 (c). Compared to STT switching, which has a latency of a few ns, the SOT mechanism offers a faster switching scheme. Furthermore, the SOT efficiency is not subjected to a limited spin polarization but is proportional to the spin Hall angle (SHA) and the dimensions of the spin Hall layer as presented in the equation below

$$I_{\mathrm{s}} = \theta_{\mathrm{SH}} \frac{L}{t} \frac{\hbar}{2e} I_{\mathrm{c}}. \tag{1.4}$$

Here L is the length and t is the thickness of the SOT track. In principle, SHA of a material can exceed the value of one, which enables highly efficient SOT performance. This feature of the SOT-MRAM also reserves rooms for future scalability.

In conclusion, the next generation of non-volatile memories relies on the SHE and ISHE with highly efficient charge-to-spin and spin-to-charge conversions. On the right of Figure 1.15, we show a vision of a new memory hierarchy for the next 10 - 20 years. Within this dissertation, we will focus on developing technologies focusing on the top level - SOT-MRAM and the bottom level - SOT reader for beyond 4 Tb/in^2 HDD.

1.5.3 Spin Hall materials

Identifying materials with a large SHA is a crucial topic in the development of SOT magnetic storage devices. Currently, these devices widely use HMs due to their CMOS compatibility and high electrical conductivity. However, HMs are well-known for their small SHA, which is incapable of providing high SOT efficiency. Indeed, SOT-based devices have underperformed compared to their expectations. As shown in Figure 1.17 [48], a Pt-based reader with CoFe as the FM layer gave a small output of only $R_{\mathrm{ISH}} \approx 0.2\ \Omega$ at a size of 60 nm x 65 nm. The tiny SHA of Pt $\theta_{\mathrm{SH}} = 0.08$ [49] accounts for this poor performance, which is insufficient to serve in magnetic reader applications. Hence, by integrating another material with a larger SHA, the output signal and the SNR can be enhanced.

Regarding SOT-MRAM applications, HMs have greatly contributed to achieving high-performance SOT-MRAM. β-phase W, which possesses the larger SHA of 0.4 than that of Ta and Pt, has been used in the SOT-MRAM development on a 300-mm wafer with the CMOS process as shown in Figure 1.18. In 62-nm devices, this SOT-MRAM displays high endurance over 5x10^{10} times, a sub-ns switching time of 280 ps, and power consumption of 350 fJ/bit [50]. However, for cutting-edge AI computing, which requires a few fJ/bit to keep operating energy to a minimum [51], the HM-based SOT-MRAMs need help from other technologies, like voltage-control magnetic anisotropy or toggle spin torque, to lower their writing energy to approximately 10 fJ/bit [52, 53]. Thus, more material engineering efforts

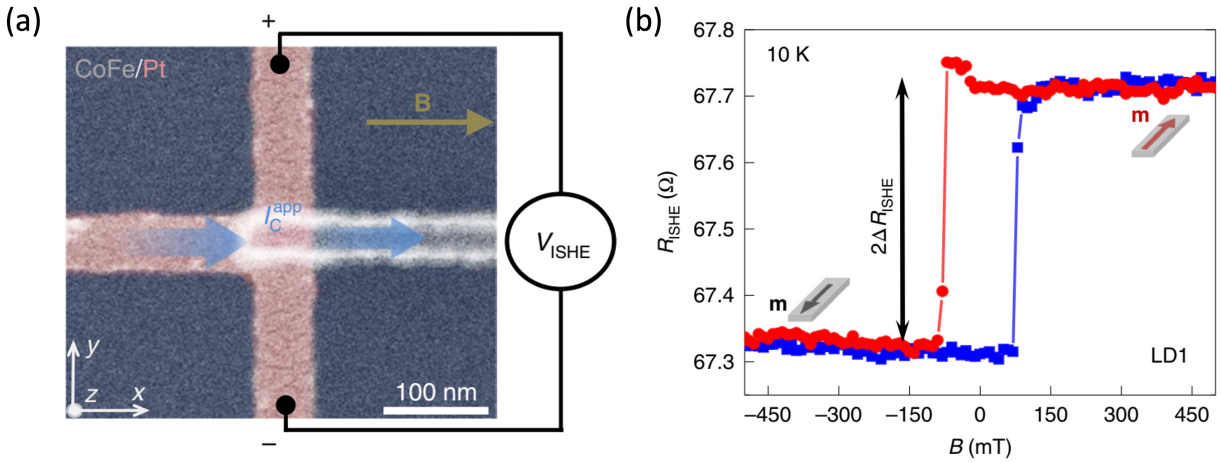

Figure 1.17: Pt-based SOT reader at the size of 60 nm × 65 nm: (a) Scanning electron microscopy (SEM) image of the Pt-based SOT reader. (b) Output signal R_{ISH} as a function of in-plane external magnetic field. Images reproduced with permission of the rights holder, Springer Nature.

should be implemented to further reduce the energy consumption. In the next chapter, we will present the fundamental principles in spintronic devices and the promising quantum materials for futuristic SOT applications.

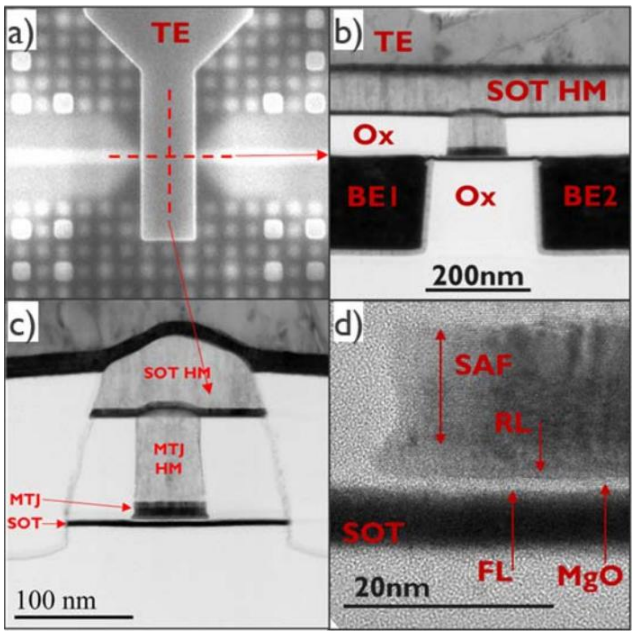

Figure 1.18: SEM image of W-based SOT-MRAM fabricated by CMOS process on a full scale 300 mm Si wafer. Images reproduced with permission of the rights holder, IEEE.

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Chapter 2: Fundamental physics of spin-orbit interaction

In this chapter, we present the background physics of spin-related phenomena. The later half of this chapter focuses on topological insulators (TIs) and especially the alloy BiSb.

2.1 Spin-orbit coupling

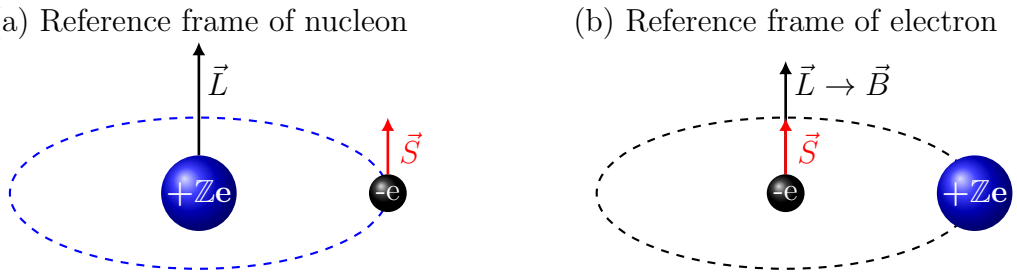

Figure 2.1: An illustration of spin-orbit coupling: (a) In the reference frame of nucleon, the electron moves around the nucleon and feels an electric field $\vec{E}$. (b) In reference frame, the electron sees the nucleon moving around it and feels a relativistic magnetic field $\vec{B}$.

Spin-orbit coupling (SOC) is the interaction between an electron's spin and its orbital motion around the nucleus. It comes from relativistic effects, where an electron experiences a magnetic field in its reference frame because it moves through the nucleus's electric field $\vec{E}$. An illustration for the SOC is shown in Figure 2.1. This interaction is especially significant in materials with heavy elements, such as heavy transition metals like Pt, Au, and heavy elements like Bi, where high atomic numbers generate a large effective electric field near the nucleus. The coupling strength is proportional to the fourth power of the atomic number,

$\mathbb{Z}^4$ [1]. The magnetic field $\vec{B}$ exhibited in the rest frame of the electron can be expressed as

$$\vec{B} = \frac{\mu_0 \mathbb{Z} e}{4\pi r^3} \vec{r} \times \vec{E}. \tag{2.1}$$

As a result, the corresponding Hamiltonian when electron's spin experiences this magnetic field is given by

$$\hat{H} = \lambda \vec{L} \vec{S}, \tag{2.2}$$

where λ is the SOC strength, $\vec{L}$ and $\vec{S}$ are the orbital angular momentum and spin angular momentum of the electron, respectively [2].

SOC strength can induce unique features in different materials. In weak SOC systems, the long spin diffusion lengths create an environment that is highly efficient for spin transport. A typical example is graphene, showing a spin diffusion length of up to a few tens of micrometers [3]. In HMs with strong SOC, it induces spin splitting in conduction bands, allowing for phenomena such as the SHE and Rashba-Edelstein effect (REE). Especially in TIs, much stronger SOC is sufficient to invert the band structure, creating an insulating bulk with gapless, spin-polarized surface states that are protected by time-reversal symmetry. Later in this chapter, we will discuss the details of TIs and why they are appealing compared to HMs.

2.2 Rashba-Edelstein effect

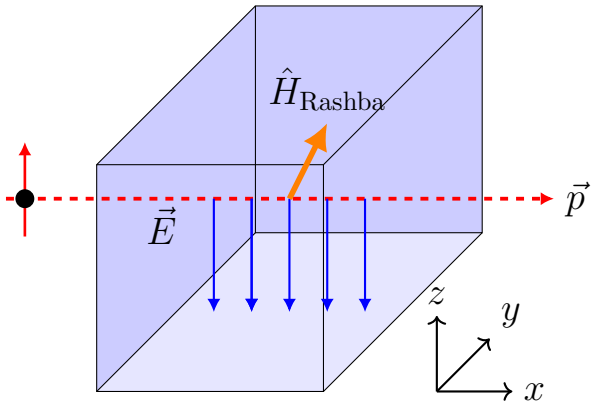

Figure 2.2: An illustration of Rashba field in a broken symmetry system.

The Rashba effect is a spin-orbit interaction (SOI), which happens in broken inversion symmetry systems, like surfaces or interfaces. In these systems, electrons feel an asymmetric electric field $\vec{E}$ perpendicular to their trajectory, creating an effective magnetic field $\vec{B}$ in their reference frame, which interacts with their spin as shown in Figure 2.2. This interaction leads to a momentum-dependent splitting of spin states, commonly described by the Rashba Hamiltonian:

$$\hat{H}_{\text{Rashba}} = \frac{\alpha_{\text{R}}}{\hbar}\left(\vec{E} \times \vec{p}\right) \cdot \sigma, \tag{2.3}$$

where α_{R} is the strength of the Rashba SOC while $\vec{p}$ and σ are the electron momentum vector and Pauli matrices, respectively. As a result, the spin degenerancy is broken and create an equilibrium state with zero net spin density as shown in the left panel of Figure 2.3.

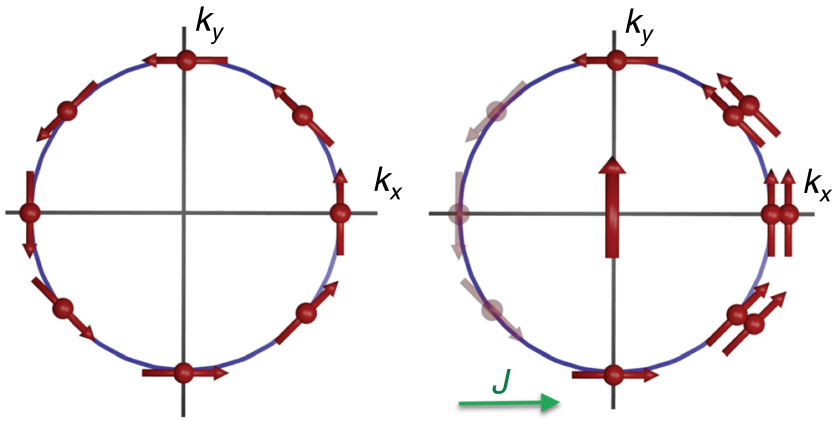

Figure 2.3: Rashba spin texture for one of the chiral states without applied electric field (left panel) and with applied electric field (right panel) [4]. Images reproduced with permission of the rights holder, Springer Nature and American Physical Society.

The REE builds upon the Rashba effect by applying a bias current. Under Rashba SOC, this current induces a nonequilibrium spin polarization due to spin-momentum locking, creating a net spin density. Such an effect can be used to create spin accumulation. As shown in the right panel of Figure 2.3, the spin polarization is perpendicular to the electron trajectory. This effect is an approach to converting charge current to a spin current where the external electric field polarizes spins in the system through the Rashba interaction [4].

2.3 Berry phase

The Berry phase concept is introduced in the context of a system in a cyclic adiabatic field. A non-degenerate quantum state can return to the initial state itself when finishing the cycle, but gains an additional phase. This phase is called Berry phase, which shows the ability to memorize the trajectory of particles [5]. Mathematically, we can illustrate such a system with a Hamiltonian $H(R)$ in a time-evolution parameter space $R(t)$. The eigenstates $|n(R)\rangle$ for this system are described as

$$H(R)\,|n(R)\rangle = \epsilon_n(R)\,|n(R)\rangle\,. \tag{2.4}$$

Noticeably, Equation (2.4) is linearly homogeneous, which allows us to specifically assign a phase factor. Thus, an additional time-dependent phase factor in R-space, is introduced to determine the eigenstates $|n(R)\rangle$. Afterwards, the time-dependent eigenstates can be written as:

$$|\psi_n(t)\rangle = \exp\left[i\gamma_n(t)\right] \exp\left\{-\frac{1}{\hbar}\int_0^t \epsilon_n\left[R(t')\right] dt'\right\}. \tag{2.5}$$

In this equation, the second exponential term is the dynamical phase factor while the first exponential term is the newly acquired Berry phase γ_n during the adiabatic process. This phase can be determined by applying $\langle n(R(t))|$ after plugging $|\psi_n(t)\rangle$ in to the time-dependent Schrödinger equation. Under Berry's description of the cyclic evolution along a closed path, the Berry phase is given by

$$\gamma_n = \oint dR \cdot A_n(R), \tag{2.6}$$

where $A_n(R)$ is called Berry connection or Berry vector potential, determined by

$$A_n(R) = i\langle n(R(t)) \left|\frac{\partial}{\partial R}\right| n(R)\rangle. \tag{2.7}$$

This equation suggests that while the individual Berry connection may change depending on the chosen phase for the wavefunctions at different point, the Berry phase itself remains unchanged in a closed loop. This key feature of Berry phase is call gauge invariant [6]. From the mathematical expression in Equation (2.6), Berry phase indeed shares analogies to gauge

field theories and differential theory. In a similar manner, a new quantity - Berry curvature $B_n(R)$ is presented, resembling a magnetic field in electrodynamics

$$B_n(R) = \nabla_R \times A_n(R). \tag{2.8}$$

Equation (2.8) implies an effective magnetic field in R-space. Specifically, in the context of spin transport in material, this effective field scatters spins in different directions, which induce an anomalous velocity. This behavior is considered as the intrinsic origins of the SHE in NM materials and anomalous Hall effect (AHE) in magnetic materials.

2.4 Anomalous Hall effect

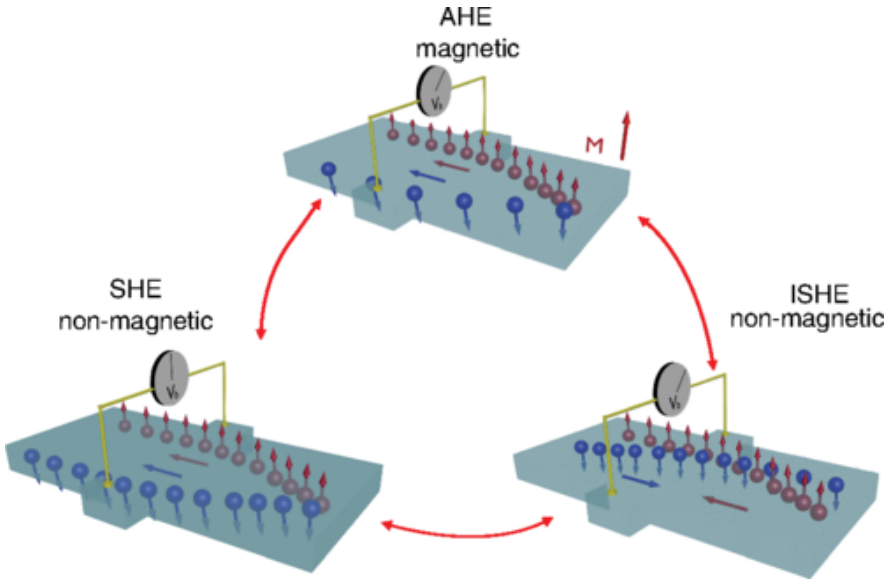

Figure 2.4: A summary of spin-dependent Hall effects including AHE, SHE, and ISHE [4]. Images reproduced with permission of the rights holder, American Physical Society.

The AHE occurs in FM materials that exhibit broken time-reversal symmetry, resulting in the generation of a Hall voltage that is perpendicular to the applied current, independent of any external magnetic field [7]. The schematic of the AHE is shown in the top panel of Figure 2.4. The Hall resistivity ρ^{xy}_{Hall} in the FM with AHE can be described as:

$$\rho^{xy}_{\text{Hall}} = \alpha_0 B + \alpha_{\text{AHE}} M, \tag{2.9}$$

where B, M, α_0, and α_{AHE} are the external magnetic field, the magnetization of the FM material, the ordinary Hall and the anomalous Hall coefficients, respectively. Thanks to its sensitivity to the magnetization, AHE is often utilized as an approach to evaluate the magnetic anisotropy of the FM materials. Unlike the classical ordinary Hall effect, the origins of AHE lie in complex quantum phenomena, including SOC, Berry curvature, skew scattering, and side jump. These mechanisms also account for other significant phenomena, SHE and ISHE, which are the main drives of this dissertation.

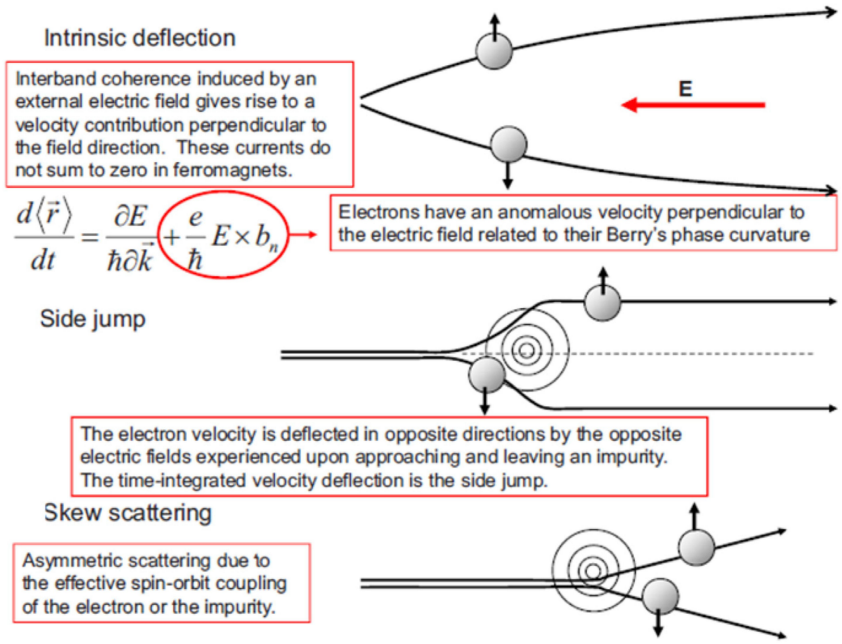

Figure 2.5: An illustration of the three main mechanisms accounted for the AHE and SHE [7]. Images reproduced with permission of the rights holder, American Physical Society.

2.5 Spin Hall effect and inverse spin Hall effect

The SHE occurs in NM materials with SOC. Rather than producing a Hall voltage, the SHE generates a pure spin current perpendicular to the applied electric field. In the absence of net magnetization, time-reversal symmetry is maintained, indicating that electrons with opposite spins are deflected in opposing directions due to SOC. This leads to spin

accumulation at the margins of the sample without generating a net charge current in the transverse direction, which is known as "pure spin current" [4]. The schematic of the SHE is shown in the bottom left of Figure 2.4. Meanwhile, the ISHE converts a spin current to a charge current as shown in the bottom right of Figure 2.4. The spin Hall angle, representing the conversion efficiency, is expressed as

$$\theta_{\mathrm{SH}} = \frac{\sigma_{xy}^{\mathrm{Hall}}}{\sigma_{xx}}, \tag{2.10}$$

where $\sigma_{xy}^{\mathrm{Hall}}$ is the spin Hall conductivity and σ_{xx} is the conductivity along the direction of bias current.

The spin Hall conductivity can be decomposed into intrinsic and extrinsic contributions, which can be expressed as:

$$\sigma_{xy}^{\mathrm{Hall}} = \sigma_{xy}^{\mathrm{intr}} + \sigma_{xy}^{\mathrm{sj}} + \sigma_{xy}^{\mathrm{ss}}. \tag{2.11}$$

Here $\sigma_{xy}^{\mathrm{intr}}$ is the contribution from the intrinsic Berry-phase mechanism while $\sigma_{xy}^{\mathrm{ss}}$ and $\sigma_{xy}^{\mathrm{sj}}$ are the spin Hall conductivity arising from the extrinsic mechanisms – skew scattering and side jump, respectively.

Intrinsically, the SOC gives rise to spin-dependent splitting. When an electric field is applied to generate a charge current, electrons experience anomalous velocity and are deflected from the original trajectories. This behavior is a result of an effective electromagnetic field created by the electric field and Berry curvature.

The other contributions are classified as extrinsic factors because they are the results of scattering events by impurities. In skew scattering, electrons, in their reference frame, are deflected by the SOC-generated relativistic magnetic field of the impurities. Depending on the alignment between spin and the effective magnetic field, electrons are likely to be scattered asymmetrically off the impurities in one direction over the opposite. As a result, a transverse current arose in the context of the AHE and the SHE.

Another extrinsic scattering mechanism is side jump. In this scattering event, electrons experience transverse displacement, leading to a net lateral shift relative to their initial trajectories. Different from skew scattering, this transverse motion is not due to asymmetrical scattering but instead results from a symmetric spin-dependent displacement at each

scattering event. When electrons are approaching the impurities, the SOC field exerts a perpendicular displacement, which shifts the electrons with different spin polarities oppositely without any bias direction. Hence, a transverse current is also observed via this mechanism. Figure 2.5 summarizes the intrinsic and extrinsic contribution to the AHE and SHE.

The SHE and the ISHE in a NM/FM junction play a significant role in spintronic device applications. Indeed, the SHE is widely used for the SOT-MRAM devices while the ISHE is applied to the SOT reader. In the next section, we will discuss the charge-to-spin and the spin-to-charge conversions by SHE and ISHE in a NM/FM junction.

2.6 Spin to charge conversion in non-magnetic and ferromagnetic junction

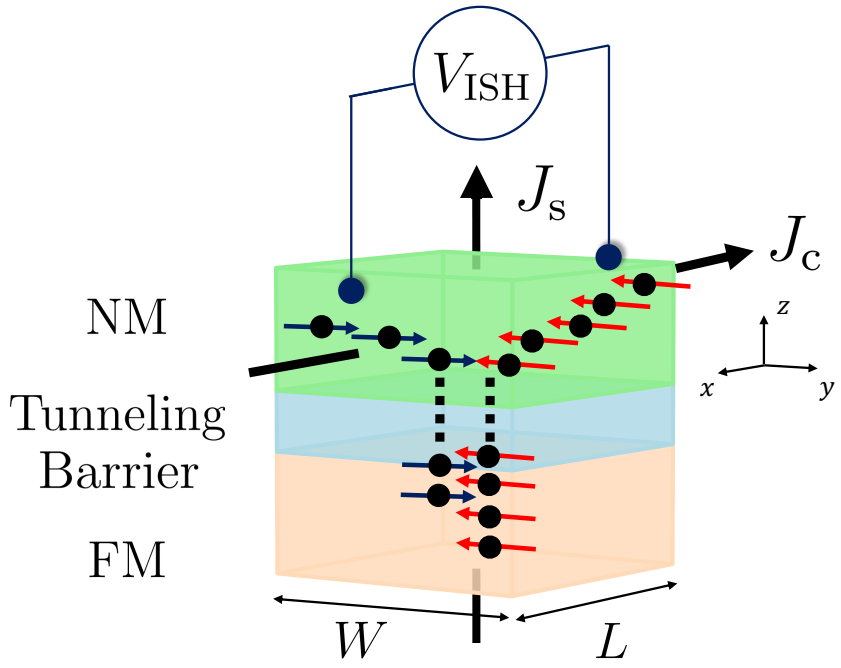

Figure 2.6: An illustration of spin transport in NM/tunneling barrier/FM junction.

In this part, we provide the analytical description of the phenomenon that a spin-polarized current is injected from the FM layer and then is transported into the NM layer.

Consider a junction made of FM/tunneling barrier/NM with the geometry parameter W and L as denoted in Figure 2.6. We set the coordinate with $z = 0$ at the interface between NM and the tunneling barrier. To begin with, a charge current is applied between the top and the bottom to generate a spin-polarized current which then tunnels through the insulating barrier and starts to diffuse in the NM via ISHE. The polarity of the charge current follows the relation $\vec{j_c} \propto \left(\vec{j_s} \times \vec{\sigma}\right)$. Inside the NM the spin-dependent chemical potential $\Delta\mu$ is governed by 1D steady-state spin diffusion equation along the z–direction [8]:

$$\frac{\partial^2 \Delta\mu}{\partial z^2} - \frac{\Delta\mu}{\lambda_{\mathrm{sf}}^2} = 0. \tag{2.12}$$

The solution for Equation (2.12) can be written as:

$$\Delta\mu = A \exp\left(\frac{z}{\lambda_{\mathrm{sf}}}\right)) + B \exp\left(-\frac{z}{\lambda_{\mathrm{sf}}}\right), \tag{2.13}$$

where A and B are the coefficients which can be determined by the continuity of the spin current and the boundary condition:

$$\frac{\partial \Delta\mu}{\partial z}|_{z=0} = -j_{\mathrm{s}}^0 \rho_{\mathrm{NM}}, \tag{2.14}$$

$$\frac{\partial \Delta\mu}{\partial z}|_{z=t_{\mathrm{NM}}} = 0, \tag{2.15}$$

with j_{s}^0 is the spin-polarized current density at the interface. Equation (2.14) expresses the continuity of the spin-polarized current at the interface whereas Equation (2.13) ensures there is no spin current at the top surface of the NM layer. Solving these equations yield the z-dependent chemical potential at the interface:

$$\Delta\mu(z) = \rho_{\mathrm{NM}} j_{\mathrm{s}}^0 \lambda_{\mathrm{sf}} \frac{\cosh[(t_{\mathrm{NM}} - z)/\lambda_{\mathrm{sf}}]}{\sinh(t_{\mathrm{NM}}/\lambda_{\mathrm{sf}})}. \tag{2.16}$$

Next, the z–dependent spin current density is calculated via:

$$j_{\mathrm{s}}(z) = -\frac{1}{\rho_{\mathrm{NM}}} \frac{\partial \Delta\mu}{\partial z} = j_{\mathrm{s}}^0 \frac{\sinh[(t_{\mathrm{NM}} - z)/\lambda_{\mathrm{sf}}]}{\sinh(t_{\mathrm{NM}}/\lambda_{\mathrm{sf}})}. \tag{2.17}$$

In the context of the ISHE, a spin current is converted into a charge current, which can be expressed by:

$$j_{\mathrm{c}}(z) = \theta_{\mathrm{SH}} \frac{2e}{\hbar} j_{\mathrm{s}}(z). \tag{2.18}$$

The average charge current density across the NM layer is obtained through:

$$\langle j_c \rangle = \frac{1}{t_{NM}} \int_0^{t_{NM}} j_c(z) dz = \theta_{SH} \frac{2e}{\hbar} \frac{\lambda_{sf}}{t_{NM}} \tanh\left(\frac{t_{NM}}{2\lambda_{sf}}\right) j_s^0. \tag{2.19}$$

Eventually, the inverse spin Hall voltage across the interface of NM is governed by:

$$V_{ISH} = E_y L = \langle j_c \rangle \rho_{NM} L = \frac{\theta_{SH} P \rho_{NM}}{W} \frac{\lambda_{sf}}{t_{NM}} \tanh\left(\frac{t_{NM}}{2\lambda_{sf}}\right) I, \tag{2.20}$$

with $j_s^0 = \frac{\hbar}{2e} P \frac{I}{WL}$. Equation (2.20) is the essence in the SHE tunneling spectroscopy [9] and will be applied in Chapter 4 for the SOT reader.

2.7 Charge to spin conversion in non-magnetic and ferromagnetic junction

In this section, we examine a charge-to-spin conversion by either SHE or REE in a trilayer of NM/insertion layer/FM trilayer.

2.7.1 The influence of the insertion layer on spin transportation

First, we consider the effect of the insertion layer on the measured spin Hall angle in the trilayer. The insertion layer can be either a NM metallic or insulating material with weak SOI. By considering the contribution of the insertion layer, one can write the θ_{SH} as:

$$\theta_{SH} = \frac{J_s}{J_c} = T_{isrt} \theta_{SH}^{intr}, \tag{2.21}$$

where $0 \leq T_{isrt} \leq 1$ represents the spin transparency of the insertion layer while the θ_{SH}^{intr} is the intrinsic spin Hall angle of the NM layer, which is determined by the quality of the fabricated material. By integrating a perfect insertion layer without spin loss $T_{isrt} \approx 1$, such as the case of Pt/NiO/Co [10], the measured θ_{SH} can approach the intrinsic value. Equation (2.21) suggests that θ_{SH} can be improved by high-quality spin current source with large θ_{SH}^{intr} and by integrating high T_{isrt} insertion layer.

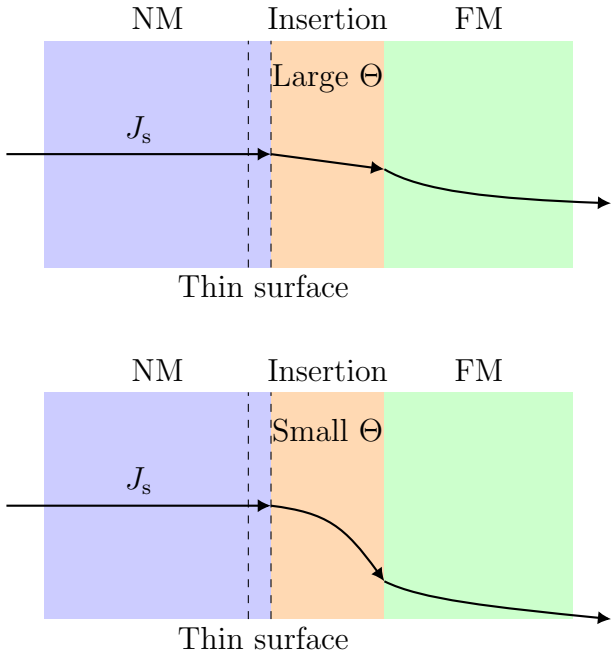

Figure 2.7: An illustration of the spin current transparency and Θ_{SH}.

Now, let us consider the spin accumulation on a 2D surface of a 2D NM, in contact with an insertion layer as shown in Figure 2.7. The charge-to-spin conversion can be written as

$$\theta_{SH} = \frac{t_{NM}}{2}\Theta_{SH}, \tag{2.22}$$

with $t_{NM}/2$ is the thickness of NM that involves in creating spin accumulation at the interface. The newly added Θ_{SH} can be interpreted as a 2D spin Hall angle covering physics of the 2D interface rather than the conventional 3D spin Hall angle θ_{SH}. When the NM is a TI, Θ_{SH} is given by [11]:

$$\Theta_{SH} = \frac{1}{v_F(\tau_t + \tau_{sf})}, \tag{2.23}$$

with v_F is the Fermi velocity of electron and τ_t, τ_{sf} are the tunneling/diffusion and spin-flip scattering time constants, respectively. When a charge current is applied to the NM, the spin-polarized electrons need to overcome the spin potential at the interface, and then diffuse into the insertion layer. This process involves the tunneling/diffusing process represented by τ_t and the spin-flip scattering process represented by τ_{sf}. In the trilayer setup, the insertion layer is usually much thinner than its spin diffusion length λ_{sf}. As a result, the spin-flip

scattering events occur at the insertion/FM interface instead of in the bulk of the insertion layer. Thus, one can treat the spin potential as a step function in the insertion/FM junction and the τ_{sf} is replaced by an effective τ_{mix}. This effective time constant τ_{mix} represents the time for spins to be flipped/transferred across the insertion/FM junction. A shorter τ_{mix} can allow more efficient spin current injection. Furthermore, the effective τ_{mix} is characterized by the quality of the insertion/FM junction and can be expressed via spin-mixing conductance $g_{\mathrm{mix}}^{\uparrow\downarrow}$:

$$\tau_{\mathrm{mix}} = \frac{\pi \hbar D_{\mathrm{s}}}{g_{\mathrm{mix}}^{\uparrow\downarrow}}, \tag{2.24}$$

where D_{s} is the density of state of the insertion layer at Fermi level. In a practical situation, $g_{\mathrm{mix}}^{\uparrow\downarrow}$ can be replaced by an effective $g_{\mathrm{eff}}^{\uparrow\downarrow}$:

$$g_{\mathrm{eff}}^{\uparrow\downarrow} = \frac{4\pi M_{\mathrm{s}} t_{\mathrm{FM}}}{g\mu_{\mathrm{B}}} \left(\alpha - \alpha_{\mathrm{FM}}\right), \tag{2.25}$$

with $(\alpha - \alpha_{\mathrm{FM}})$ is the enhanced damping constant between that of the full stack and the FM only. This enhancement can be probed by spin-torque ferromagnetic resonance measurement.

To conclude this section, the Θ_{SH} factor can be regarded as the extrinsic factor to achieve a large charge-to-spin conversion. Θ_{SH} not only considers the diffusion/tunneling process but also takes the characteristic of the insertion layer/FM interface into account. Hence, it defines two approaches to improve the spin Hall angle: using a proper insertion layer with short τ_{t} for fast spin transport and depositing a high quality insertion layer/FM interface with high spin-mixing conductance $g_{\mathrm{mix}}^{\uparrow\downarrow}$. An illustration of the relationship between Θ_{SH} and the interfacial spin transparency is summarized in Figure 2.7.

2.7.2 Dynamics of the magnetization

In this section, we will discuss the dynamics of the magnetization under the interaction with a spin current in the context of STT-MRAM and SOT-MRAM. Throughout this section, we will explain the reason why SOT-MRAM is considered as the successor of STT-MRAM with lower latency and energy consumption.

2.7.2.1 Landau–Lifshitz–Gilbert equation

In a FM/NM junction, the dynamics of the magnetization $\vec{m}$ of the FM layer is governed by the LLG equation:

$$\frac{\partial \vec{m}}{\partial t} = -\gamma \vec{m} \times H_{\mathrm{k}} + \alpha \vec{m} \times \frac{\partial \vec{m}}{\partial t}. \tag{2.26}$$

The first term in this equation represents the precession of the magnetization around its anisotropy field while the second term stands for the Gilbert damping mechanism with damping constant α. In principle, one can decide materials with appropriate α. Depending on the applications. For instance, in the spin torque and spin Hall oscillator, a weak damping is preferrable for the magnetization precession where as in the SOT-MRAM application, a strong damping can enhance the switching speed.

2.7.2.2 Spin-transfer torque

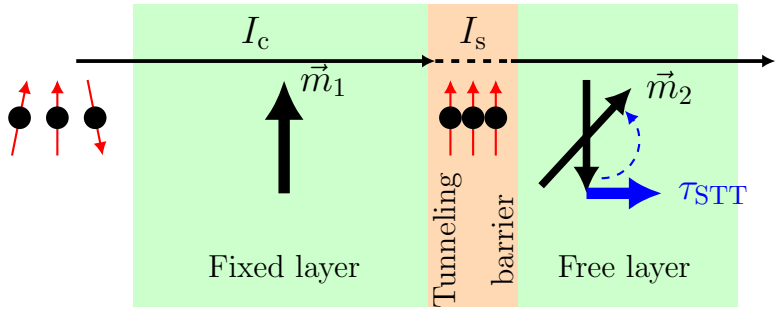

Figure 2.8: An illustration of the STT effect on the magnetization of free layer.

In the STT-MRAM, a bias charge current I is injected into the MTJ pillar to generate a spin-polarized current I_{s}. This I_{s} generates STT that can flip the magnetization $\vec{m}_2$ of the free layer. The dynamics of $\vec{m}_2$ is described by adding an STT term into Equation (2.26) [12]:

$$\frac{\partial \vec{m}_2}{\partial t} = -\gamma \vec{m}_2 \times H_{\mathrm{k}} + \alpha \vec{m}_2 \times \frac{\partial \vec{m}_2}{\partial t} + \gamma \mu_0 \frac{\hbar I P}{2e M_{\mathrm{s}} V_2} \vec{m}_2 \times (\vec{m}_2 \times \vec{m}_1), \tag{2.27}$$

with $\vec{m}_1$ is the magnetization of the fixed layer. Noticeably, the newly added torque drives $\vec{m}_2$ away or toward the direction of $\vec{m}_1$, and is collinear to the direction of the Gilbert damping torque. Thus, to complete a switching, the STT torque must be larger than the

damping torque. With the cancellation of the Gilbert damping torque by the STT torque, we qualitatively expect the relatively long precession of the magnetization before reaching the equillibrium. An illustration for this STT mechanism is shown in Figure 2.8. From this mechanism, it is possible to express the dynamics of the magnetization at the switching event as

$$\alpha\vec{m_2} \times \frac{\partial\vec{m_2}}{\partial t} = -\gamma\mu_0\frac{\hbar IP}{2eM_sV}\vec{m_2} \times (\vec{m_2} \times \vec{m_1}), \tag{2.28}$$

$$\gamma\mu_0\frac{\hbar}{2e}IP\partial t = \partial m_2 M_s V \tag{2.29}$$

By solving Equation (2.28) expressing the torque equilibrium, the threshold switching current $I_{\text{threshold}}$ of the STT effect is expressed as:

$$I_{\text{threshold}} = \frac{2e}{\hbar}\alpha\frac{M_sV}{P}H_k \tag{2.30}$$

On top of that, Equation (2.29) is the expression of the conversation of angular momentum where the change of magnetization ∂m equals to the angular momentum provided by the flow of spin-polarized current. Thus, the latency of the STT switching can be expressed by

$$\frac{\partial m}{\partial t} = \gamma\mu_0\frac{\hbar IP}{2eM_sV}. \tag{2.31}$$

Obviously, for a fixed volume of a specific FM material, the threshold switching current and the latency significantly depend on the bias I and the spin polarization of the FM material. Unfortunately, the latter is always less than 1 creating an obstacle on the path to achieve ultrafast and ultralow power operation for STT-MRAM.

2.7.2.3 Spin-orbit torque

In SOT-MRAM, an in-plane charge current is applied to the spin Hall layer to create a perpendicular pure spin current that can manipulate the magnetization $\vec{m}$ of the free layer. Equation (2.26) can be modified as:

$$\frac{\partial\vec{m}}{\partial t} = -\gamma\vec{m} \times H_k + \alpha\vec{m} \times \frac{\partial\vec{m}}{\partial t} - \gamma H_{AD}\vec{m} \times (\vec{m} \times \vec{\sigma}) - \gamma H_{FL}\vec{m} \times \vec{\sigma}. \tag{2.32}$$

Here, there are two SOT terms are added: the antidamping-like component $\vec{m} \times (\vec{m} \times \vec{\sigma})$ and the field-like component $\vec{m} \times \vec{\sigma}$.

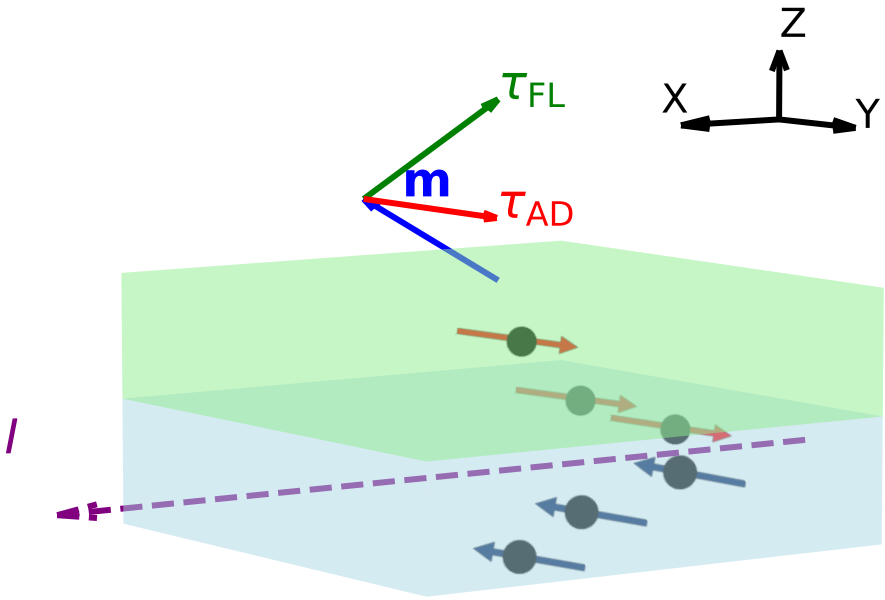

Figure 2.9: Illustration of the effect of field-like torque and antidamping-like torques on the magnetization. For simplicity, we only show the spin current source and the FM free layer.

For simplicity, here we consider a FM layer with a perpendicular magnetic anisotropy (PMA) effective field along the z direction. With such a configuration, the field-like torque, which is aligned in the (xy) plane, tends to tilt the torque towards the in-plane direction. Thus, it does not support the deterministic switching but instead increasing the threshold switching current [13]. On the contrary, the antidamping-like torque is the driving mechanism in this case. Noticeably, a significant difference between STT and SOT is that the antidamping-like torque is directed along $\vec{m} \times (\vec{m} \times \vec{\sigma})$ and is not collinear to the Gilbert damping torque. This nature of the antidamping-like torque almost eliminates the precession of the magnetization during switching event, which reduces the latency. As soon as the pure spin current supplies sufficient torques, an abrupted switching occurs [14]. However, since $\vec{m}$ is in z direction, the antidamping-like torque can only stochastically switch $\vec{m}$ to $-z$ or z. Without an in-plane external magnetic field H_{x} to break the symmetry, it is not possible to achieve the deterministic switching. Other solutions have been proposed to eliminate the use of an additional bias magnetic field such as using the AFM and synthetic AFM couplings or canted insertion layer that can break the symmetry internally [15]. In a system with

negligible field-like term, the threshold switching current density under the macrospin model is given by [16]:

$$J_{\mathrm{th}} = \frac{2e}{\hbar}\frac{M_{\mathrm{s}}t_{\mathrm{FM}}}{\theta_{\mathrm{SH}}}\left(\frac{H_{\mathrm{k}}}{2} - \frac{H_{\mathrm{x}}}{\sqrt{2}}\right). \tag{2.33}$$

This equation suggests that using spin Hall material with large θ_{SH} can reduce the threshold switching current density. Researchers have been actively searching for such a candidate for years and have found that TIs - quantum materials with strong SOC can have a θ_{SH} much larger than 1.

2.8 Topological insulators

In this section, we will discuss the essential properties of TIs, which makes them appealing candidates for spin Hall materials. We also focus on BiSb – a conductive TI, which is the main material in this dissertation.

2.8.1 Band inversion

In an insulator, the energy difference between the valence and conduction bands, referred to as the band gap, is sufficiently high to prevent electrons from being excited from the valence band to the conduction band. In metals, the valence and conduction bands overlap, resulting in an undefined band gap. This overlap guarantees the continual availability of electrons for conduction. In contrast to conventional materials, TIs represent a novel category of exotic materials that cannot be categorized as either pure insulators or metals. Within the material's bulk, the valence and conduction bands are delineated by the band gap; however, at the surface, these bands are interconnected by metallic states, referred to as topological surface states (TSSs). This unique feature of TIs is a result of the strong SOC that inverts the band structure as shown in Figure 2.10.

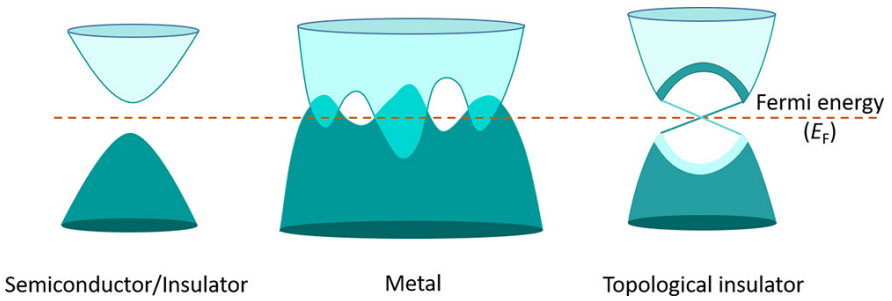

Figure 2.10: An illustration of band structure of semiconductor/insulator (left), metal (center) and TIs (right) [17]. Reprinted with permission from American Chemical Society.

2.8.2 Topological surface states

The TSSs are the most important feature of TIs, which locates at the surfaces for 3D TIs. The TSSs are protected by time-reversal symmetry (TRS), which means that they are robust against any NM perturbations. This protection is necessary because any deviation from the TSSs would violate TRS, which is only possible through magnetic interference. The Dirac cone at a TSS, which has a spin-momentum locking relationship, prevents impurity backscattering and thus preserves electron coherence.

On top of that, the Berry phase, which encapsulates the geometric properties of the electron wavefunctions, plays a pivotal role in TIs. A non-trivial Berry phase of π is associated with the TSSs, causing the electronic wavefunctions to exhibit a non-zero Berry curvature in momentum space [18]. This curvature maintain spin-polarized currents without impurities scattering. Combining with the topological protection, both provides a highly efficient spin-momentum locking and corresponding helicity. Figure 2.11 summarizes features of TIs such as band structure and Dirac cone of a 2D TI (panel (a)), 1D edge state of a 2D TI (panel (b)), 2D surface states of a 3D TI (panel (c)) and the corresponding 2D Dirac cone (panel (d)) [19].

Thanks to these superiorities, TIs are favorable to produce the colossal SHE that clearly distinguishes it from other HMs. Thus, the θ_{SH} in TIs is expected to be much larger than that in HMs.

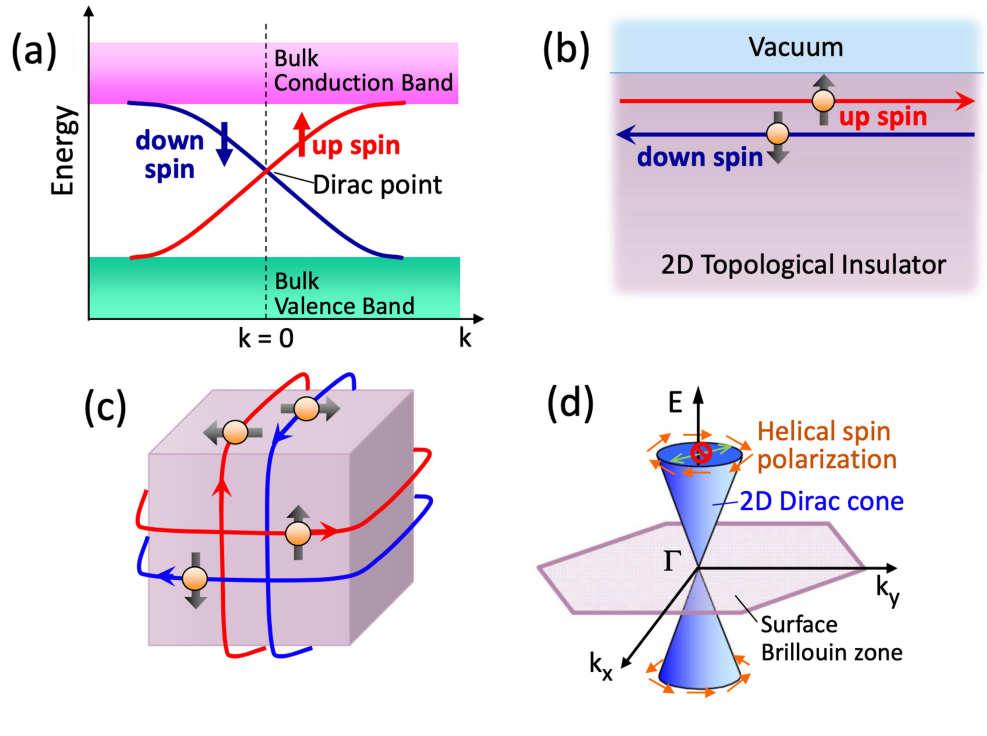

Figure 2.11: Prominent features of TI: (a) Band structure of a 2D TI with a 1D Dirac cone. (b) Helicity in the 1D edge state of a 2D TI. (c) Illustration of helicity in the 2D surface states of a 3D TI. (d) 2D Dirac cone. Image reproduced with permission of the rights holder, Journal of the Physical Society of Japan.

2.8.3 Recent progress in 3D topological insulators

Following the observation of edge states in 2D-TI HgTe-based quantum wells [20], the observation of 2D surface states of 3D TI [21] has attracted attention. Furthermore, giant θ_{SH} was observed in Bi_2Se_3 [22] and $(Bi_{0.5}Sb_{0.5})Te_3$ [23]. Their θ_{SH} is at least one order higher than that of HM. Even though promising θ_{SH} have been reported among those TIs, the low electrical conductivity ($\sigma \approx 10^4\ \Omega^{-1}\ m^{-1}$) is a huge barrier to prevent further practical application of TIs to spintronics. To serve in spintronic applications such as SOT-MRAM, TIs need to be integrated with other metallic FM layers whose $\sigma \approx 10^5\ \Omega^{-1}\ m^{-1}$. In this situation, shunting current into other layers rather than TIs is unavoidable, which limits the

charge-to-spin conversion efficiency of TIs. Hence, a TI material with large θ_{SH} as well as high electrical conductivity is essential to achieve further progress. Table 2.1 summarizes θ_{SH} and σ among popular HMs and TIs. It is worth noticing from this table that BiSb stands out from other candidates with gigantic θ_{SH} together with high σ. Hence, the remained parts of this chapter will focus on the introduction of BiSb and the ongoing progress.

Type	**Material**	$\theta_{\mathbf{SH}}$	σ (Ω^{-1} $\mathbf{m}^{-1}$)
HM	β-Ta [24]	0.15	5.3×10^5
	β-W [25]	0.4	4.7×10^5
	Pt [14]	0.08	4.2×10^6
TI	Bi_2Se_3 [22]	2-3.5	5.7×10^4
	Bi_xSe_{1-x} [26]	18.8	7.8×10^3
	BiSb [27]	52	2.5×10^5

Table 2.1: An overview of SHA and conductivity of some TIs and HMs.

2.8.4 BiSb topological insulator

2.8.4.1 Theoretical prediction and first observation

The topological state of BiSb with inversion symmetry was predicted by using $\mathbb{Z}_2$ invariant model proposed by Fu and Kane [28, 29]:

$$(-1)^{\nu} = \prod_i \delta_i, \tag{2.34}$$

where $\delta_i = \prod_{n=1}^{N} \xi_{2n}(\Gamma_i)$. Here $\xi_{2n}(\Gamma_i) = \pm 1$ is the parity eigenvalue of the $2n$-th Γ_i energy band that has the Kramers pair degeneracy $\xi_{2n} = \xi_{2n} - 1$. For 3D TIs, there are four Z_2 invariant ν_i with $i = 0, 1, 2, 3$. Among them, ν_0 is called the strong invariant, which classify TIs into strong or weak topological phase. Through this model, the alloy $Bi_{1-x}Sb_x$ with $0.07 < x < 0.22$ (shaded region in Figure 2.12 (a)) yields strong TI properties. A year later, by using angle-resolved photoemission spectroscopy technique, the TSSs of BiSb were

observed, marking the first observation of a 3D TI [30]. Figure 2.12 (b) shows a surface where electrons with different spin polarity flow in opposite direction around the Γ point. In addition, a π Berry phase is also confirmed from the full Fermi-surface data. However, due to its very small band gap of < 20 meV and complicated band structure, BiSb had been less attractive than other second generation of 3D TIs like Bi_2Se_3, Bi_2Te_3, and Sb_2Te_3 until BiSb is recognized as a conductive TI with a giant SHE.

2.8.4.2 BiSb with giant spin Hall effect

Unlike other TIs, BiSb has a high carrier mobility approximately 10^4 $\mathrm{cmV^{-1}s^{-1}}$ giving it a high bulk conductivity of $4 \sim 6.4 \times 10^5\,\Omega^{-1}\mathrm{m}^{-1}$. Indeed, BiSb grown by molecular beam epitaxy (MBE) has been reported to possess a giant intrinsic $\theta_{\mathrm{SH}} = 52$ while maintaining highly conductive surface states [27]. A tunable σ_{BiSb} with respect to BiSb thickness ranging from $\sigma_{\mathrm{BiSb}} \approx 1 \sim 4 \times 10^5\ \Omega^{-1}\ \mathrm{m}^{-1}$ for thin films thinner than 25 nm and $\sigma \approx 4 \sim 6.4 \times 10^5$ $\Omega^{-1}\ \mathrm{m}^{-1}$ for thin films thicker than 80 nm [31]. Figure 2.12 (a) shows the summary of σ_{BiSb} as a function of thickness and Sb concentration. The colossal θ_{SH} of BiSb is attributed for the TSSs of BiSb (012) rhombohedral structure with four Dirac cones at $\bar{\Gamma}$, $\bar{M}$, $\bar{X}_1$, and near $\bar{X}_2$ [32], [33].

2.8.4.3 Recent progress and challenges

Although this finding has brought BiSb closer to many practical applications, the preliminary work on BiSb was done by MBE, which is incompatible with mass production. Fabrication of BiSb using industry-friendly tool such as magnetron sputter is preferred. Several efforts have been conducted to achieve the feasibility of BiSb for industrial applications:

1. On c-plane sapphire: Large $\theta_{\mathrm{SH}} = 10.7$ has been reported on highly textured sputtered BiSb (110) in junction with PMA Co/Pt [34].

2. Silicon substrate compatibility: $\theta_{\mathrm{SH}} \approx 3$ has been observed on oxidized silicon substrate [35, 36]. Obviously, there is a significant drop in θ_{SH} due to the fact that BiSb remains as polycrystalline.

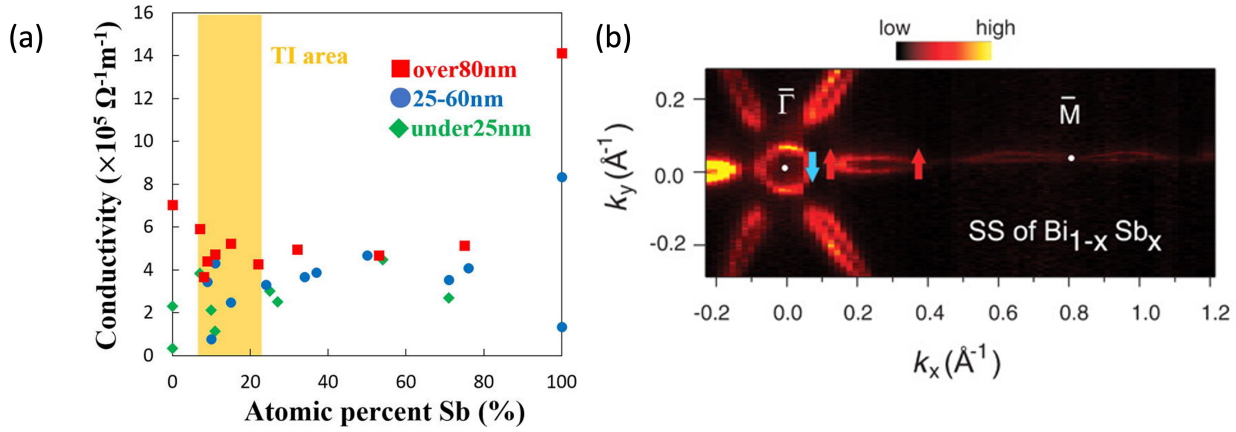

Figure 2.12: (a) BiSb conductivity from various $Bi_{1-x}Sb_x$ samples with different thickness and Sb concentration at 270K. [31] (b) Observation of surface states of BiSb at Fermi energy using spin-integrated angle-resolved photoemission spectroscopy [30]. Image reproduced with permission of the rights holder, AIP Publishing and The American Association for the Advancement of Science, respectively.

3. Nanosecond SOT magnetization switching: Ultrafast operation of BiSb has been demonstrated using nanosecond DC pulse. The threshold switching current density was kept as low as 1.7×10^7 A/cm^2 at 1 ns [36].

4. High temperature capability: There is a rising concern whether BiSb can maintain its superior SHE at high temperature. Indeed, a relative large $\theta_{SH} \approx 4.9$ was reported in BiSb at 125°C. Another work has proved the high-temperature resilience of sputtered BiSb on c-plane sapphire by post annealing up to 250°C while preserving an impressive $\theta_{SH} = 6.0$ [37].

5. High TMR ratio: Sputtered BiSb-MTJ has displayed a TMR ratio of 90% in the in-plane MTJ which proves the potential integration of BiSb for realistic SOT-MRAM [38].

These works have drawn a promising future for the integration of BiSb with spintronic devices. However, there are several challenges need to be addressed:

1. Sb diffusion: There are reports that when sputtering BiSb, Sb significantly breaks free from Bi bonding and migrates into the FM layers as shown in Figure 2.13. Such a decomposition not only damages the PMA effective field but also degrades the intrinsic θ_{SH} of BiSb. The Sb diffusion creates a blockage to achieve high bit density and ultralow power performance. Inserting a metallic diffusion barriers with a good spin transparency to suppress the diffusion of Sb can preserve θ_{SH} intrinsically but there is a concern on shunting current.

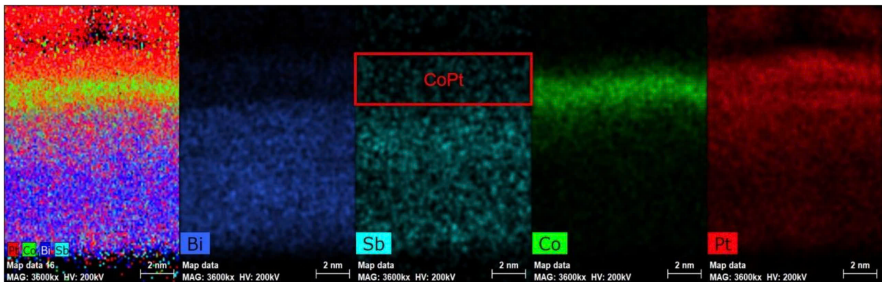

Figure 2.13: EDX mapping of sputtered BiSb in junction with Co and Pt. Image reproduced with permission from author of [39].

2. Shunting: The development so far has coupled BiSb with other metallic materials such as Ru, Ti, Pt, which results in current shunted into the conductive metals. Highly resistive oxide materials, such as NiO, with spin current transparency are possiblle candidates as demonstrated in [40].

3. Single-phase sputtered BiSb on oxidized silicon substrate: Previous studies have suggested a relationship between BiSb crystal quality and the large θ_{SH}. However, to obtain manufacturability, amorphous Si/SiO_x substrate is preferred where sputtered BiSb remains in multiple phases. A solution is the insertion of buffer and seed layers to enhance the crytallinity of BiSb.

4. CMOS compatibility: SOT-MRAM can be integrated to CMOS electronics by the back-end-of-line (BEOL) process which includes high temperature approximately 400°C. Despite preserving relative large $\theta_{SH} = 6.0$ after 250°C annealing process, the low

melting point of BiSb at approximately 280°C still prevents the integration with current manufacturing CMOS process. A popular solution is sputtering BiSb on on top of the MTJ in the final deposition process to avoid high temperature exposure.

Thoughout this dissertation, we will proposal several solutions to tackle the mentioned challenges to move closer to the integration of BiSb topological insulator for magnetic storage devices.

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Chapter 3: Sample preparation and characterization techniques

3.1 Sample preparation

3.1.1 Magnetron sputter

Magnetron sputtering is a deposition technique employing high-energy ions from gaseous plasma to knock off atoms from the surface of a target. As a result, knocked-off atoms can travel through a vacuum environment and deposit onto a substrate, forming a thin film. Figure 3.1 shows the typical structure of a sputtering machine. At first, the chamber is

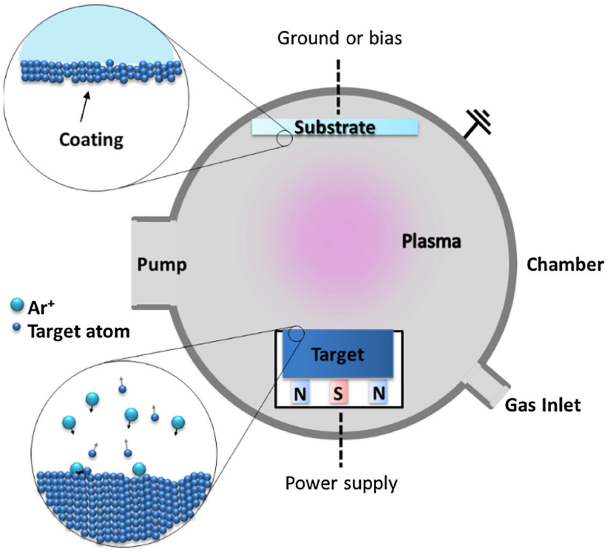

Figure 3.1: Schematic of magnetron sputter [1]. Images reproduced with permission of the rights holder, Elsevier.

pumped to an ultra-high vacuum state to suppress the partial pressure of background gases

and to eliminate potential contaminants. After achieving a base pressure, a noble gas, such as Ar, Kr, Xe. is injected into the chamber to increase the pressure up to the range of 0.1 Pa - 1.0 Pa. High voltage across the anode and the cathode is applied to ionize sputter gas and generate a plasma state near the surface of the target. Optionally, one may introduce typical reactive gases such as O_2 and N_2 to induce chemical reactions that change the pure target material surface into a surface with already reacted molecules. This process is called reactive sputtering, which allows sputtering compounds without the pure compound targets.

Typically, the cathode is located behind the target while the anode is connected to the chamber as electrical ground. Electrons in the sputtering gas are detached by such a strong electric field, allowing positive atoms to accelerate towards the negatively charged cathode. Thus, a high-energy collision happens at the surface of the target, ejecting the atoms out of the surface. Because of strong collision, ejected atoms have sufficient kinetic energy to reach the substrate. The magnet at the cathode can localize the electrons in the plasma state close to the surface of the target. This confinement allows a higher density of plasma and a faster deposition rate, and it also avoids damage due to collisions between electrons and the substrate.

Figure 3.2 shows a schematic picture of our sputtering system for thin films preparation and the annealing process. We equip each grow chamber with non-reactive Ar and reactive O_2 gas, to diversify our material capability. Samples can be transferred between chambers via an ultra-high vacuumed tunnel. A combination of turbo-molecular pumps (TMPs) and rotary pumps (RPs) maintains all chambers at below 1×10^{-6} Pa.

3.1.2 Hall bar fabrication process

Within this dissertation, we employ two techniques, either a lift-off process or an ion milling process, to pattern the Hall bar devices for electrical and spin transport measurement. We adopted the lift-off process to fabricate the SOT reader in Chapter 4 thanks to its compatibility with the design, while the ion milling process can reserve large bare films for multiple purposes, such as Hall bar fabrication, X-ray diffraction (XRD) analysis, supercon-

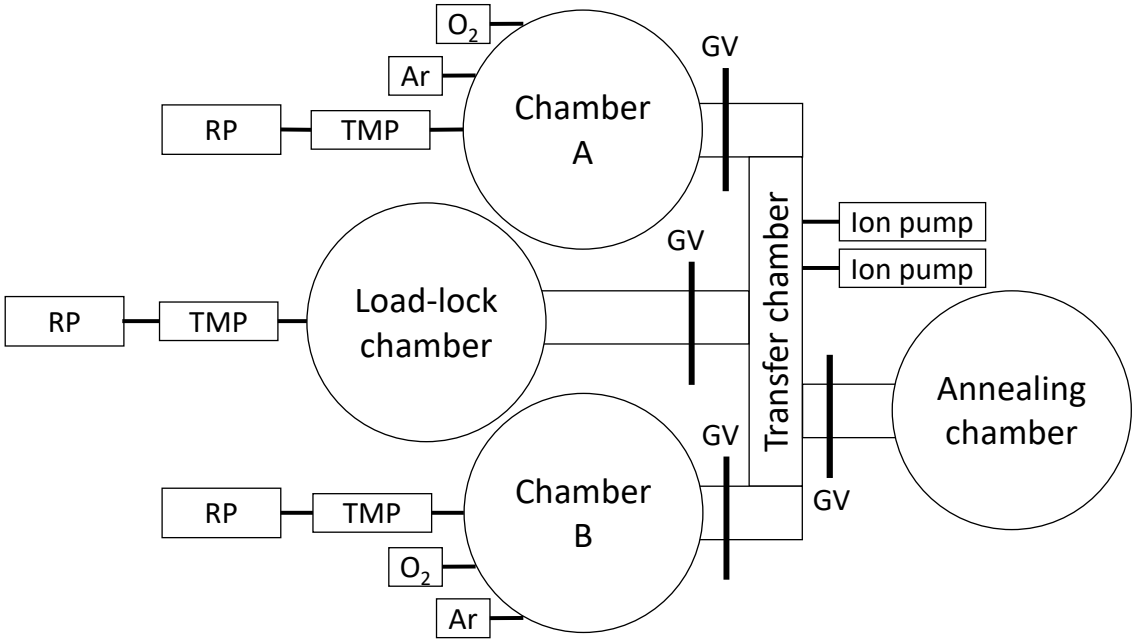

Figure 3.2: A schematic of our sputtering system: All growth chambers are at ultra high vacuum with base pressure below 1×10^{-6} Pa.

ducting quantum interference device (SQUID), and transmission electron microscopy (TEM) used in Chapter 5 and 6.

3.1.2.1 Lift-off process

Figure 3.3 shows an illustration of a lift-off process consisting of five steps:

- Coating: Substrate is coated with a lift-off resist PMGI-SF6, followed by a hard bake at 150°C for 5 minutes. Then, another layer of a positive photoresist OFPR is coated onto the substrate prior to 110°C bake for 2 minutes. Two layers of photoresist allow easier lift-off after depositing materials.

- Exposure: Coated substrate is exposed using a desktop maskless optical lithography system PALET DDB-701 to pattern 20 μm × 60 μm Hall bars.

- Development: The substrate is developed in NMD-3 developer for 45 seconds and is rinsed with deionized water to completely remove residual photoresist.

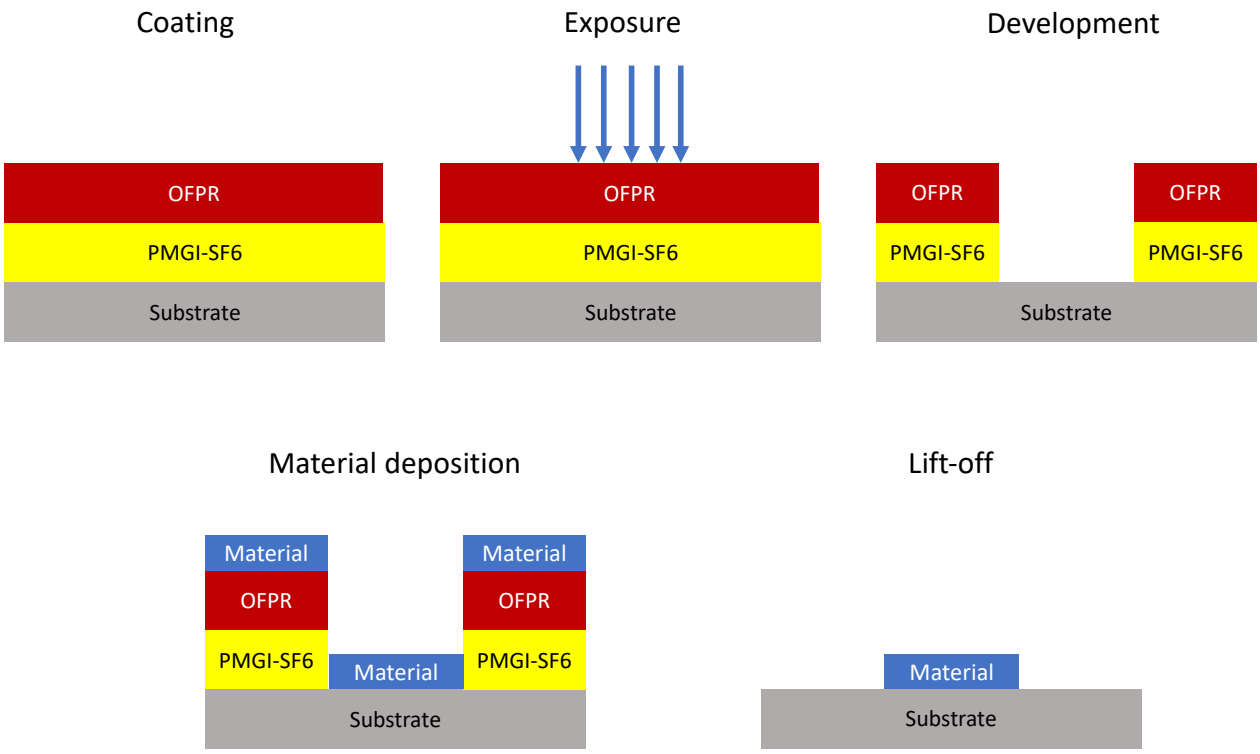

Figure 3.3: A diagram illustrates the fabrication process of Hall bars using the lift-off process.

- Material deposition: Thin films are deposited using magnetron sputtering.
- Lift-off: Residual material can be removed by dipping samples into Striper-104 at 130°C for 12 minutes.

3.1.2.2 Ion milling process

Figure 3.4 shows an illustration of a ion-milling process consisting of five steps:

- Material deposition: Thin films are deposited using magnetron sputtering.
- Coating: The substrate is coated with OFPR and then is soft baked at 110°C for 2 minutes.

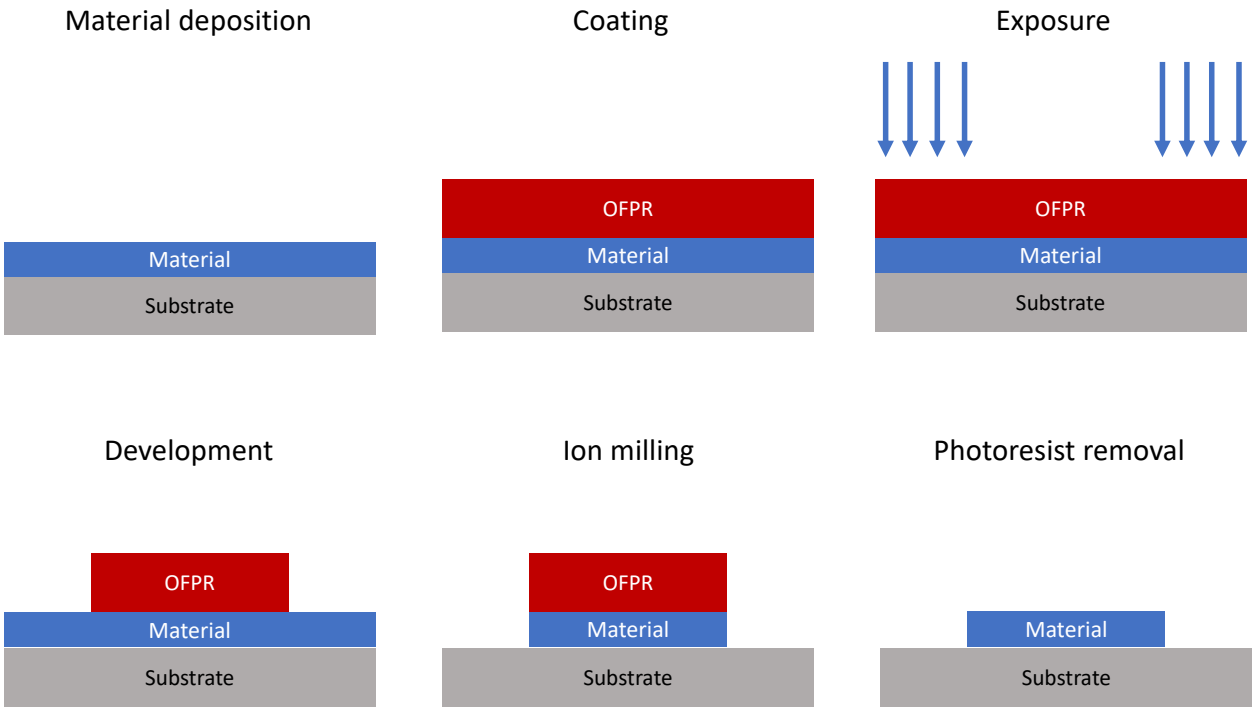

Figure 3.4: The illustration depicts the process of fabricating Hall bars using the ion milling process.

- Exposure: Unlike in the lift-off process, here the exposure areas are those need to be removed by ion milling.
- Development: Similar to the lift-off process, the samples are developed in NMD-3 developer for 45 seconds and later is rinsed with deionized water.
- Ion milling: Sample are under dry etching with an incident angle of 60° until the oxide surface of the substrates is revealed.
- Photoresist removal: Residual material can be removed by dipping samples into Striper-104 at 130°C for 12 minutes.

After patterning the Hall bar devices via either the lift-off or ion milling process, completed

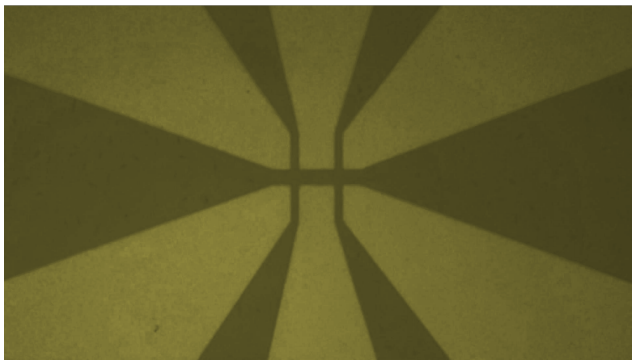

Figure 3.5: An optical image of completed Hall bar device.

Hall bar devices can be obtained. An optical image of the Hall bar device is shown in Figure 3.5 as an example.

3.2 Magnetization measurement

To obtain the magnetization M of samples, the SQUID is employed. Based on the Josephson effect, SQUID can measure extremely weak magnetic moments. Figure 3.6 shows the schematic of the measurement system MPMS from Quantum Design. A SQUID capsule located at the bottom of the rod is connected to a gradiometer regarded as detection coil. The magnetization can induce a current flowing in the detection coil. Eventually, the magnetization of the sample can be evaluated via the output voltage, which is proportional to the detection coil's current.

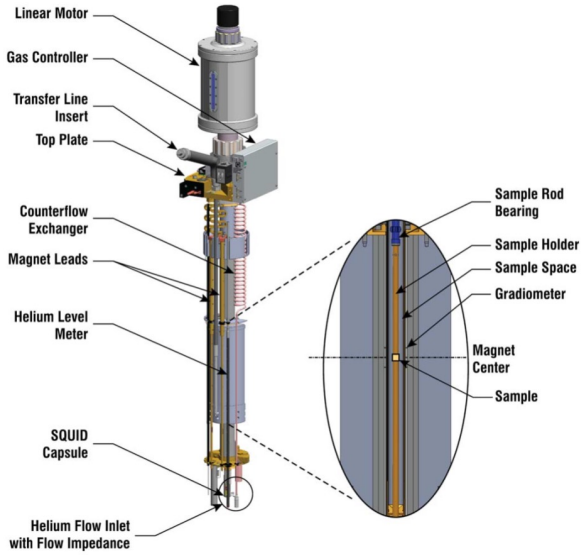

Figure 3.6: The schematic diagram of the SQUID magnetometer MPMS [2]. Images reproduced with permission of the rights holder, IEEE.

3.3 X-ray spectroscopy

X-ray spectroscopy techniques are essential tools in materials science, providing detailed insights into the structural and physical properties of thin films. In this dissertation, we use XRD and X-ray reflectivity (XRR) to analyze crystal structures and thin film thicknesses, respectively.

3.3.1 X-ray diffraction

XRD is a prevalent technique for examining the crystalline structure of thin films. It quantifies the diffraction of X-rays by the periodic atomic planes within a crystal, disclosing essential information regarding phase composition and crystallographic orientation. The diffraction condition is governed by Bragg's Law:

$$n\lambda = 2d\sin\theta, \tag{3.1}$$

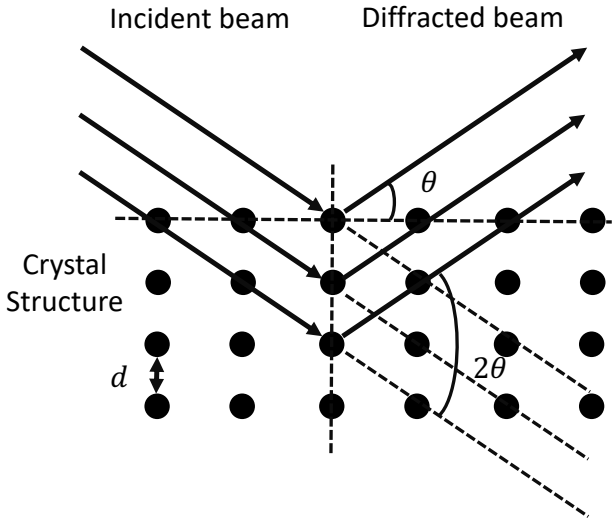

Figure 3.7: A schematic of X-ray diffraction governed by Bragg's Law.

in which n is the order of reflection, λ is the X-ray wavelength, d is the interplanar spacing, and θ is the diffraction angle. Figure 3.7 demonstrates the Bragg's Law with the visualization of parameter d and θ. By determine the interplanar spacing of a crystal structure, one can estimate the location of the diffraction peaks of each material. For example, BiSb crystallizes in a rhombohedral structure with lattice constants of $a = 4.54$ Å and $c = 11.86$ Å. The interplanar spacing of a rhombohedral structure is given by:

$$\frac{1}{d^2} = \frac{4}{3}\left(\frac{h^2 + k^2 + hk}{a^2}\right) + \frac{l^2}{c}, \tag{3.2}$$

where h, k, and l are the Miller indices of the plane. By plugging Equation 3.2 into 3.1, the peak positions of (012) and (003) plane of BiSb are located at $2\theta = 27.22^o$ and 22.52^o, respectively when using Cu Kα X-ray with $\lambda = 1.54$ Å.

After collecting the XRD spectrum, the orientation of a thin film can be identified by examining the locations and intensities of diffraction peaks. A random polycrystalline film generates peaks corresponding to many crystallographic planes, whereas a textured or orientated film displays intensified peaks linked to particular planes.

Furthermore, the peaks in XRD spectrum can provide information on the grain size G

through the Scherrer equation:

$$G = \frac{K\lambda}{\beta \cos\theta}. \tag{3.3}$$

In this equation, K is the dimensionless shape factor with a typical value of 0.9 while β is the FWHM of the peak.

3.3.2 X-ray reflectivity

XRR is a method employed to measure the thickness, density, and surface/interface roughness of thin films. It depends on the reflection of X-rays from the interfaces between each layer in the film. In this work, we employed XRR as a technique to determine sputtering rates for various materials.

XRR measures the intensity of reflected beam as a function of a small incident angle θ. The interference between reflected beams from the film surface and the interfaces creates an oscillatory pattern in the reflectivity spectrum. The periodicity of these oscillations is directly related to the film thickness. To do so, one needs to extract a normalized oscillation, which is a function of thickness t, from the reflectivity spectrum [3]

$$\cos\left(\frac{4\pi t}{\sqrt{\sin^2\theta - 2\delta}}\right), \tag{3.4}$$

with δ is the reflective index of the layer. The thickness of the layer can be determined by locating the peak position in the Fourier transform spectrum of the normalized oscillation. An example of how to determine the thickness of a thin film is shown in Figure 3.8.

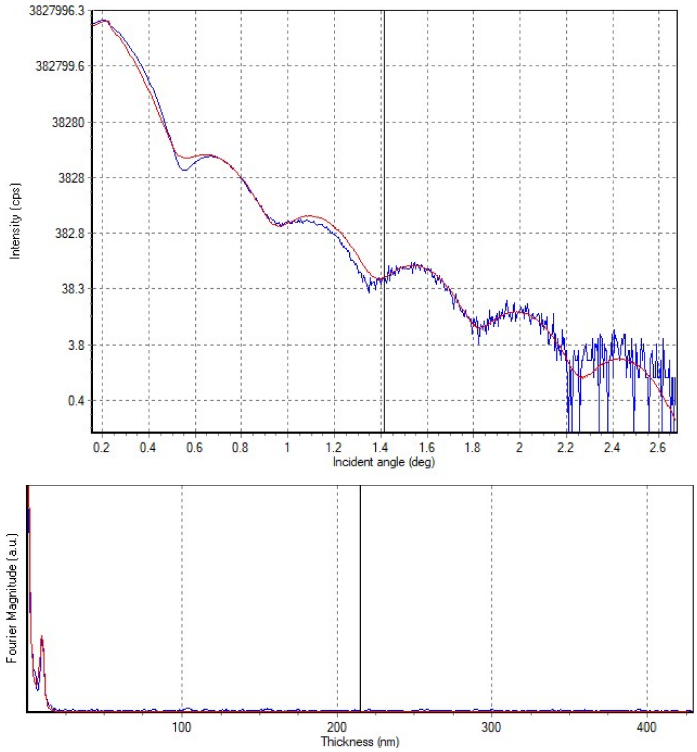

Figure 3.8: An example of a XRR spectrum of a single layer thin film shows the unnormalized oscillation pattern (top) and its Fourier transform of the normalized oscillation (bottom).

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[2] D. Hurt, S. Li, and A. Amann, "Versatile SQUID Susceptometer With Multiple Measurement Modes," *IEEE Transactions on Magnetics*, vol. 49, no. 7, pp. 3541–3544, Jul 2013.

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Chapter 4: Integration of BiSb topological insulator for a spin-orbit torque reader in magnetic recording technology beyond 4 Tb/in^2

A SOT reader employing the ISHE has recently been proposed as a next-generation sensor for magnetic recording technologies beyond 4 Tbit/in^2. Nevertheless, SOT readers employing the HMs exhibit a small output voltage and a low SNR attributable to the limited spin Hall angles of these materials. In this chapter, we demonstrate the integration of BiSb TI with strong ISHE into the SOT reader that can significantly improve the output voltage and SNR. First, in Section 4.1, we introduce the background and the motivation to conduct this work. Then, in Section 4.2, we theoretically calculate the noises in a 20 $\times$ 20 nm^2 BiSb-based SOT reader to establish the relationships between SNR and θ_{SH} at various bias currents which indicates the minimum requirement of $\theta_{\mathrm{SH}} = 2$ at a bias current of 400 μA. Afterwards, we demonstrate a substantial spin Hall angle of 2.6—5.1 in sputtered BiSb TI on top of various FMs with in-plane magnetization in Section 4.3. The spin Hall angle of BiSb is significantly larger than that of HMs, which paves a way to achieve the SOT reader with substantial output and elevated SNR. In particular, we discovered that a sample using CoFe/MgO/BiSb stack exhibits the largest spin Hall angle of 5.1 among others. Based on that foundation, we then demonstrate a proof-of-concept BiSb-based SOT reader using CoFe/MgO/BiSb stack. By integrating BiSb to the reader, we can increase the output voltage to 15 mV when inputing a current density of 9.4 kA/cm^2 at room temperature, which projects a giant $\theta_{\mathrm{SH}} = 61$ for BiSb. The detailed of this part is covered in Section 4.4. Overall, this work demonstrates the potential of BiSb for SOT reader for the next-generation magnetic recording technologies

beyond 4 Tb/in^2.

4.1 Introduction

In recent years, the rapid growth of data centers and cloud services has placed significant demands on HDD technology. The areal density of magnetic recording media is anticipated to surpass 4 Tb/in^2 in the near future. Achieving such an ultrahigh areal density requires a miniaturization of the magnetic read head to less than 20 nm while guaranteeing an SNR of at least 28 dB [1]. These requirements pose three significant challenges for the current TMR reader technology.

1. First, as the device size decreases, the resistance of the MTJ pillar is substantially increased. Thus, the two-terminal TMR reader experiences a significant surge in thermal noise.

2. Second, an additional STT noise arises due to the spin-polarized current flowing from the reference layer to the free layer in the MTJ [2].

3. Lastly, reducing the total thickness is difficult due to the complex structure of the MTJ.

Recently, an SOT reader based on the ISHE has been proposed as an alternative technology to address these challenges [3]. The SOT reader structure comprises two layers in minimum: an FM layer and an SOT layer, as depicted schematically in Figure 4.1. When a charge current is applied between the top and bottom shields, a perpendicular spin-polarized current is injected from the FM layer into the SOT layer. The direction of spin polarization depends on the magnetization of the FM layer, which detects the stray magnetic field from the media. The SOT layer then converts this perpendicular spin-polarized current into an in-plane charge current, generating an output voltage between the two lead terminals via the ISHE [4].

Comparing with the TMR reader, the SOT reader has three distinct advantages:

1. Unlike the TMR counterpart, which requires a magnetic reference layer and is constrained by the dimension of the reference stack, the SOT reader only requires a single FM layer, allowing for easier reduction of the total thickness.

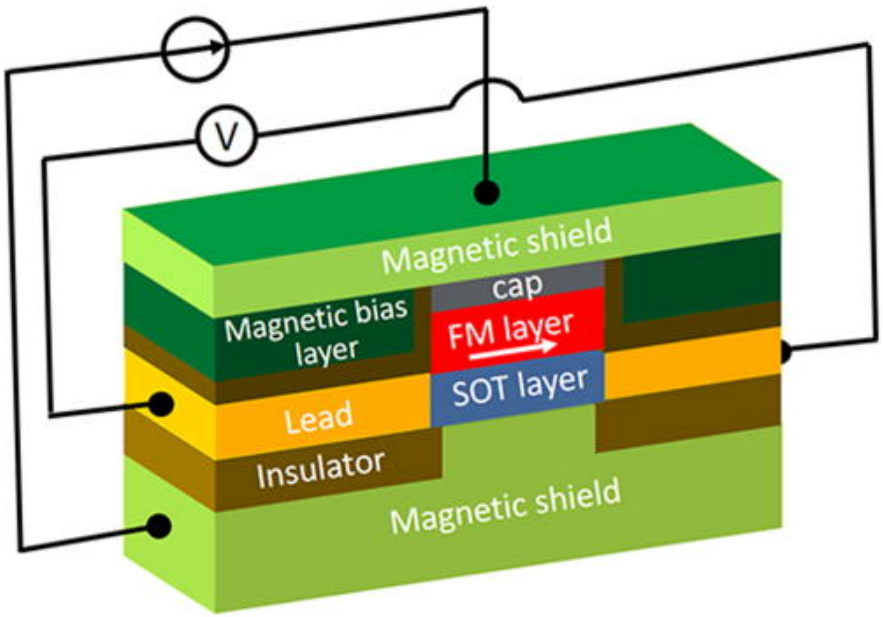

Figure 4.1: Schematic illustration of an SOT reader as viewed from a media facing surface.

2. Additionally, the SOT reader does not experience an STT noise.

3. Most significantly, the differential output voltage of the SOT reader treats thermal noise of the pillar as common-mode noise, which allows better scalability compared with the TMR reader. The detailed analysis will be covered in the next section.

However, the output voltage in devices based on HMs is typically in the range of μV, which is insufficient for realistic SOT reader applications [5], due to the relatively small spin Hall angle of HMs.

To improve the output voltage and SNR, an SOT material with a large θ_{SH} can offer a solution. In this regard, TI with a strong SOC [6, 7] such as Bi_2Se_3 [8], $(Bi, Sb)_2Te_3$ [9, 10], and BiSb [11] are under consideration. Among those TIs, BiSb has stood out with a giant θ_{SH} of 52 when grown by MBE. Furthermore, large θ_{SH} up to 10.7 was observed for sputtered BiSb in junctions with FM layers with both IMA and PMA [12, 13, 14, 15]. Hence, BiSb promises an enhancement in output voltage and SNR for the SOT reader.

4.2 Noise analysis

In this section, we investigate the possible noise contribution to the output signal of the SOT reader. Through the analysis, we establish the relationships between SNR and θ_{SH} at various bias currents.

First, as derived in Chapter 2, an output voltage V_{ISH} of an SOT reader biased by I can be expressed via [16]

$$\frac{V_{\mathrm{ISH}}}{I} = \frac{\theta_{\mathrm{SH}} P \rho_{\mathrm{SOT}} \lambda_{\mathrm{sf}}}{w_{\mathrm{SOT}} t_{\mathrm{SOT}}} \tanh\left(\frac{t_{\mathrm{SOT}}}{2\lambda_{\mathrm{sf}}}\right). \tag{4.1}$$

In this equation, the output voltage is proportional to θ_{SH} and ρ_{SOT} which can be improved further thanks to the large θ_{SH} and relatively high ρ_{SOT} of TIs. Here we introduce the modified version of Equation 4.1 to cope with the nature of BiSb TI where the in-plane charge current can flow in both bulk states and TSSs. Fortunately, for BiSb, the Fermi level is located in the bulk band gap [17, 18]. Additionally, the bulk band gap of BiSb significantly widens as the BiSb thickness decreases due to the quantum confinement effect [19], reaching approximately 200 meV at 10 nm [20] and 400 meV at 5.5 nm [21]. As a result, when the thickness of BiSb is 10 nm or less, the generated in-plane charge current predominantly flows on the 2D topological surface states of BiSb. This behavior has been experimentally verified in stand-alone BiSb thin films [19, 20, 22]. Thus, Equation 4.1 can be rewritten as

$$\frac{V_{\mathrm{ISH}}}{I} = \frac{\theta_{\mathrm{SH}} P R_{\mathrm{sheet}}^{\mathrm{BiSb}}}{w_{\mathrm{BiSb}}} \lambda_{\mathrm{sf}} \tanh\left(\frac{t_{\mathrm{surface}}^{\mathrm{BiSb}}}{2\lambda_{\mathrm{sf}}}\right). \tag{4.2}$$

To determine the requirement of BiSb spin Hall angle for SNR $\geq$ 28 dB at various bias currents, we assume a 20 nm $\times$ 20 nm SOT reader with CoFe (3 nm)/MgO (0.8 nm)/BiSb (5 nm) stack, as shown in Figure 4.2 (a). The MgO (0.8 nm) layer, although optional, can be inserted between CoFe and BiSb to enhance spin polarization and minimize intermixing between BiSb and CoFe. Additionally, the MgO layer helps reduce voltage shunting in BiSb caused by the CoFe layer. Noticeably, the total thickness of this stack is just 8.8 nm, which is considerably thinner than the 20 nm thickness requirement for achieving 4 Tb/in^2. For calculating the output voltage, we assume the following parameters: sheet

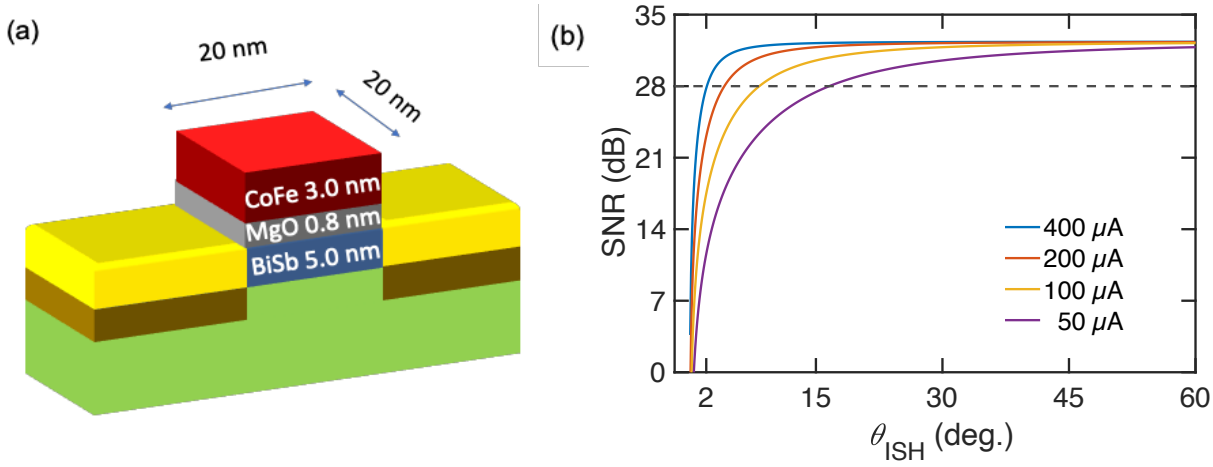

Figure 4.2: (a) Model of a 20 nm × 20 nm SOT reader with the stack of CoFe (3 nm)/ MgO (0.8 nm) / BiSb (5 nm). Some insulating layers, magnetic bias layers and top magnetic shield are omitted for simplicity. (b) Relationships between the SNR and θ_{SH} for the reader in (a) at different applied bias current I of 400, 200, 100, and 50 μA.

resistance $R_{\mathrm{sheet}}^{\mathrm{BiSb}} = 1000\,\Omega$ [20], spin diffusion length $\lambda_{\mathrm{sf}} = 2$ nm, and spin current thickness $t_{\mathrm{surface}}^{\mathrm{BiSb}} = 2$ nm for BiSb [23], with a spin polarization factor $P = 0.5$ for CoFe [24].

Next, we analyze the potential noise contributions in the BiSb-based SOT reader. Since the measured V_{ISH} represents the potential difference between the two edges of the SOT layer as depicted in Figure 4.1, thermal noise originating from the CoFe/MgO junction constitutes common-mode noise. This type of noise influences the overall electrical potential of the BiSb layer but does not impact the differential V_{ISH}. Instead, the thermal noise N_{th} arises from the sheet resistance of the BiSb layer itself. Therefore, it is calculated by:

$$N_{\mathrm{th}} = \sqrt{4k_B T R_{\mathrm{sheet}}^{\mathrm{BiSb}} f}, \tag{4.3}$$

Here, we use $T = 300$ K and $f = 1$ GHz.

Another source of noise is magnetic noise, which originates from the thermal fluctuations of the FM layer. These fluctuations affect the direction of spin polarization, thereby influencing the output voltage in a manner similar to that observed in TMR readers. The magnetic

noise voltage N_{mag} is determined by:

$$N_{\mathrm{mag}} = V_{\mathrm{ISH}} \sqrt{\frac{4\mu_0 k_B T \alpha f}{\gamma H_{\mathrm{stiff}}^2 M_{\mathrm{s}} V_{\mathrm{FM}}}}. \tag{4.4}$$

Here, we assumed that $\alpha = 0.01$, $H_{\mathrm{stiff}} = 0.1$ T, $M_{\mathrm{s}} = 1.5$ MA/m.

Lastly, amplifier noise N_{amp} must also be taken into account, which can be governed by

$$N_{\mathrm{amp}} = c\sqrt{f}. \tag{4.5}$$

Here, we assume $c = 4$ nV/$\sqrt{\mathrm{Hz}}$.

Eventually, with a utilization factor of 30% for V_{ISH}, the SNR is calculated by

$$\mathrm{SNR} = 20 \log \left(\frac{0.3\, V_{\mathrm{ISH}}}{\sqrt{N_{\mathrm{th}}^2 + N_{\mathrm{mag}}^2 + N_{\mathrm{amp}}^2}} \right). \tag{4.6}$$

Figure 4.2 (b) shows the relationships between SNR and θ_{SH} of BiSb at various applied bias currents I from 50 μA to 400 μA (equivalent to 1.25×10^7 to 1×10^8 A/cm^2). This figure suggests a general trend that SNR increases sharply with rising θ_{SH} at smaller values and then saturates at approximately 32 dB for larger θ_{SH}. This saturation can be explained by Equation 4.6; while thermal noise and amplifier noise are independent of θ_{SH}, the magnetic noise N_{mag} is proportional to V_{ISH}, making it dominant at larger θ_{SH}. As a result, the SNR reaches the saturation at higher θ_{SH} values. The required θ_{SH} for achieving SNR ≥ 28 dB depends on the bias current. For a bias current of 400 μA (1×10^8 A/cm^2), a minimum θ_{SH} of 2 is sufficient. Lowering the bias current improves the reliability of the reader but a higher θ_{SH} is necessary. Later, in Section 4.3, we introduce relatively large θ_{SH} between 2.6 and 5.1 in sputtered BiSb/FM samples with in-plane magnetization, suggesting the feasibility of using smaller bias currents down to 160 μA (or 2.5×10^7 A/cm^2). In addition to the absence of STT noise, it is important to note that the SOT reader is also robust against thermal noise. Specifically, increasing the sheet resistance R_{sheet} does not degrade the SNR, since $V_{\mathrm{ISH}} \sim R_{\mathrm{sheet}}$ while $N_{\mathrm{th}} \sim \sqrt{R_{\mathrm{sheet}}}$. This behavior contrasts with the TMR reader, where an increase in resistance leads to a reduction in SNR.

4.3 Large spin Hall angle in sputtered BiSb topological insulator on top of various ferromagnets with in-plane magnetization for SOT reader application

As suggested by the noise analysis, a minimum θ_{SH} of 2 is necessary for BiSb to serve as the SOT layer in the reader. In this section, we investigate the θ_{SH} of sputtered BiSb on top of various FM materials such as CoFeB, Co, NiFe, and CoFe with in-plane magnetization. The objective of this section is to guarantee a sufficient value of θ_{SH} to achieve large SNR.

4.3.1 Sample fabrication and measurement setup

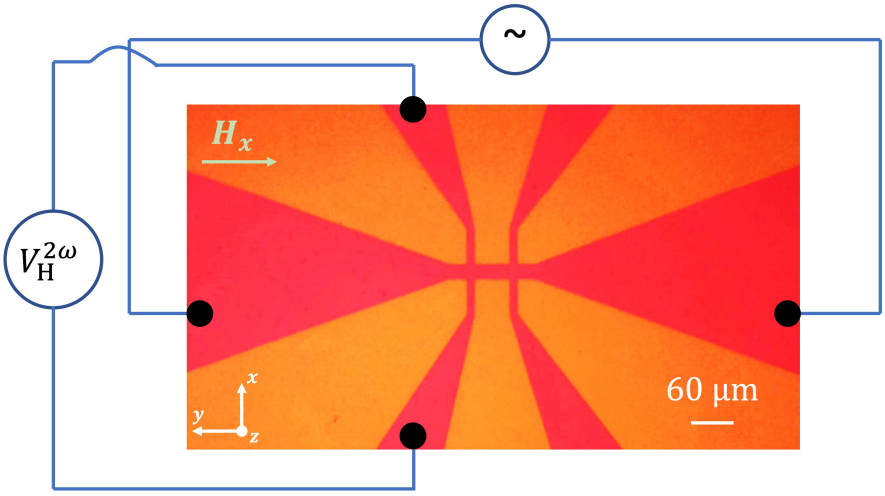

Figure 4.3: Optical image of a six-terminal Hall bar and schematic for second harmonic Hall measurement.

For θ_{SH} evaluation, we prepared multiple samples comprising BiSb thin films (top) with various FM materials deposited on surface oxidized silicon substrates. The configurations of our samples are outlined as follows: Stack A consists of BiSb (10 nm) on top, followed by Pt (1 nm), CoFeB (1 nm), and another layer of Pt (1 nm). Stack B features BiSb (10 nm) on top, with Pt (1 nm), Co (1 nm), and Pt (1 nm) beneath. Stack C includes BiSb (10 nm)

on top, followed by NiFe (1 nm) and Ru (1 nm). Finally, stack D has BiSb (10 nm) on top, followed by MgO (1 nm), CoFe (1 nm), and a buffer layer of 6 nm. The selection of CoFeB, Co, and CoFe is based on their relatively high spin polarization in conjunction with MgO, whereas NiFe was selected due to its low magnetostriction. Regarding the composition of Bi and Sb, we used $Bi_{85}Sb_{15}$ in stacks A-C while $Bi_{90}Sb_{10}$ in stack D. Stacks A and B were capped with MgO (1 nm) and Ta (1 nm), respectively, while stack C was capped with NiCu (1 nm), and stack D was capped with Ta (3 nm) and NiO (3 nm) to prevent the oxidation of the underlying BiSb layer.

Eventually, we patterned 20 μm × 60 μm Hall bars on these stacks using optical lithography for the second harmonic Hall resistance measurement. Figure 4.3 shows an optical image of a six-terminal Hall bar and the experimental setup for the second harmonic Hall measurement. In this measurement, we inject an alternating current (AC) with 259.68 Hz into the Hall bar along the x-axis. This AC current induces a perpendicular pure spin current via the SHE in BiSb. The resulting oscillating antidamping-like field H_{AD} lifts the magnetization of the FM layer out of plane, creating an orthogonal component of the magnetization. This simultaneously generates a second harmonic Hall voltage $V_{\mathrm{H}}^{2\omega}$ which can be collected by a lock-in amplifier. This measurement is conducted when scanning an in-plane H_{x}. Finally, the H_{AD} carrying information of SOT strength is extracted by fitting $R_{\mathrm{H}}^{2\omega}$ as a function of H_{x} using the equation [25]:

$$R_{\mathrm{H}}^{2\omega} = \frac{R_{\mathrm{AHE}}}{2}\frac{H_{\mathrm{AD}}}{H_{\mathrm{k}} + H_{\mathrm{x}}} + R_{\mathrm{ONE}}H_{\mathrm{x}} + R_{\mathrm{ANE+SSE}}. \tag{4.7}$$

By conducting the second harmonic Hall measurement under different bias currents, we obtained relationships between H_{AD} and J_{BiSb} which are later plugged into the following equation to determine θ_{SH}

$$\theta_{\mathrm{SH}} = \frac{2e}{\hbar} t_{\mathrm{FM}} M_{\mathrm{s}} \frac{\partial H_{\mathrm{AD}}}{\partial J_{\mathrm{BiSb}}}. \tag{4.8}$$

Noticeably, each term in Equation (4.7) has a unique dependence on the external field which allows an easy seperation of the contributions between different effects. Additionally, the first term, corresponding to the SOT field, is inversely proportional to $H_{\mathrm{k}} + H_{\mathrm{x}}$. Thus, to observe a sizable SOT effect via the second harmonic Hall resistance $R_{\mathrm{H}}^{2\omega}$, it is necessary to

reduce H_k. To do so, in stack A and B, we implemented two Pt layers sandwiching the FM layers (CoFeB and Co). The dual interfaces between Pt layers and FM layer can induce an additional PMA which help reduces the in-plane magnetic anisotropy (IMA) H_k. The spin Hall angle of Pt is small, but this sandwich structure can eliminate any artifacts caused by the parasitic SOT effect. With this configuration, the pure spin currents from the top and bottom Pt tend to cancel each other out. In stack C, H_k is sufficiently small due to the low magnetization of NiFe. In stack D, the interfacial PMA at the MgO/CoFe interface leads to a reduction in H_k.

4.3.2 Spin Hall angle characterization of samples

4.3.2.1 Sample A

Figure 4.4 (a) shows the schematic structure of stack A. The FM layer in this stack is CoFeB (1 nm) sandwiched by two Pt (1 nm) layers. Figure 4.4 (b) shows the DC anomalous Hall resistance of stack A, measured under a H_z. We obtained $R_{AHE} = 2.0\ \Omega$ and $H_k = 6.5$ kOe for this stack. Note that H_k is smaller than the demagnetizing field of CoFeB thanks to the interfacial PMA from the two Pt layers. Figure 4.4 (c) shows $R_H^{2\omega}$ as a function of H_x measured at $J_{BiSb} = 0.15,\ 0.18,\ 0.20,$ and 0.23 MA/cm^2. Figure 4.4 (d) shows the linearity of H_{AD} – J_{BiSb} obtained by fitting $R_H^{2\omega} - H_x$ curves to Equation 4.7. We obtained $\theta_{SH} = 2.6$ for stack A with $M_s = 800$ emu/cm^3 and $t_{CoFeB} = 1$ nm.

4.3.2.2 Sample B

Figure 4.5 (a) shows the schematic structure of stack B. For this stack, we also used the sandwich structure, but instead the FM was replaced by Co (1 nm). Figure 4.5 (b) shows the DC anomalous Hall resistance of stack B, measured under a H_z. We observed $R_{AHE} = 1.5\ \Omega$ which is smaller than that of stack A whereas $H_k = 6.3$ kOe shows a slight change from stack A. Figure 4.5 (c) shows $R_H^{2\omega} - H_x$ curves measured at various $J_{BiSb} = 0.14,\ 0.16,\ 0.18,$ and 0.21 MA/cm^2. Figure 4.5 (d) shows the fitted H_{AD} as a function of J_{BiSb}. With $M_s = 1000$ emu/cm^3 and $t_{Co} = 1$ nm, we achieved $\theta_{SH} = 2.8$ for stack B. The

increased M_s and reduced R_{AHE} in this stack account for the slightly increased θ_{SH}, despite $R_H^{2\omega}$ somewhat lower than that of stack A.

4.3.2.3 Sample C

Figure 4.6 (a) shows the schematic structure of stack C. In this stack, the FM layer is NiFe, which can help minimize the magnetostriction. Furthermore, NiFe is reported to induce the (012) orientation of BiSb [26], which is associated with giant θ_{SH} epitaxially grown by MBE [11]. A 1 nm Ru was deposited directly on the oxidized silicon surface as a buffer layer to protect NiFe from oxygen migration from the substrate. Figure 4.6 (b) shows the DC anomalous Hall resistance of stack C, measured under a H_z. We observed $R_{AHE} = 0.2\,\Omega$ which is an order of magnitude smaller than those of stacks A and B. Moreoever, $H_k = 4.8\,\text{kOe}$ is approximately 70% of those measured in stacks A and B which is accounted by the weak magnetization of NiFe. Figure 4.6 (c) shows $R_H^{2\omega} - H_x$ curves measured at $J_{BiSb} = 0.40,\ 0.50,\ 0.60,$ and $0.70\,\text{MA/cm}^2$. Despite the much smaller R_{AHE}, we observed similar magnitude of $R_H^{2\omega}$ to stack A and B, indicating stronger SOT effect delivered by BiSb in this stack. This statement was confirmed by a larger $\theta_{SH} = 4.8$ obtained from the extracted $H_{AD} - J_{BiSb}$ relationship in Figure 4.6 (d) using $M_s = 380\,\text{emu/cm}^3$ and $t_{NiFe} = 1\,\text{nm}$.

4.3.2.4 Sample D

Figure 4.7 (a) shows the schematic structure of stack D. In stack D, we investigated the SHE of BiSb sputtered on top of an MgO (1 nm) interfacial layer and a thin CoFe (0.8 nm) layer. In a realistic SOT reader, an efficient spin polarizer is necessary to supply a substantial spin-polarized current. Hence, it is recommended to use FM with high spin polarization like CoFe [24]. Additionally, MgO here is designed to further amplify the spin polarization of the spin-polarized current thanks to its well-known spin-filtering effect [27, 28, 29]. Also, the interfacial PMA of MgO/CoFe is also critical to reduce H_k to allow a measurable SOT term in the second harmonic Hall technique. Lastly, we also inserted a highly resistive buffer layer to enhance the crystal quality.

Figure 4.7 (b) shows DC the anomalous Hall resistance of stack D. Stack D exhibited $R_{\mathrm{AHE}} = 0.3\,\Omega$ and $H_{\mathrm{k}} = 9.0\,\mathrm{kOe}$. The low R_{AHE} in this stack is because the CoFe is thin and there is a shunting current flowing into the 6 nm thick buffer layer. H_{k} is also the largest among those of stacks A–C because of the strong M_{s} of 1500 emu/cm^3 for the high-quality CoFe layer. Figure 4.7 (c) shows $R_{\mathrm{H}}^{2\omega}$–H_{x} curves measured at $J_{\mathrm{BiSb}} = 0.28,\ 0.34,\ 0.40,$ and $0.45\,\mathrm{MA/cm^2}$. Note that the contribution of SOT term $R_{\mathrm{AHE}}\dfrac{H_{\mathrm{AD}}}{(H_{\mathrm{k}} + H_{\mathrm{x}})}$ to $R_{\mathrm{H}}^{2\omega}$ is relatively small compared with $R_{\mathrm{ANE+SSE}}$ due to the small R_{AHE} and large H_{k} in this stack. Figure 4.7 (d) shows the extracted $H_{\mathrm{AD}} - J_{\mathrm{BiSb}}$ relationship which yields a $\theta_{\mathrm{SH}} = 5.1$. This value is the largest among four stacks studied in this section. Furthermore, we note that the intrinsic θ_{SH} can be even larger. It is because the MgO (1 nm) interfacial layer is relatively thick, the pure spin current resulted from the strong SHE in BiSb can be significantly decreased before reaching the CoFe layer.

4.3.3 Summary

In this section, we obtained large θ_{SH} of 2.6 – 5.1 for BiSb deposited on top of four different FMs with in-plane magnetization: CoFeB, Co, NiFe, and CoFe. In particular, stack D consisting of BiSb (10 nm)/MgO (1 nm)/CoFe (0.8 nm)/buffer (6 nm) exhibited the largest θ_{SH} of 5.1, which has potential to provide high SNR for the SOT reader application.

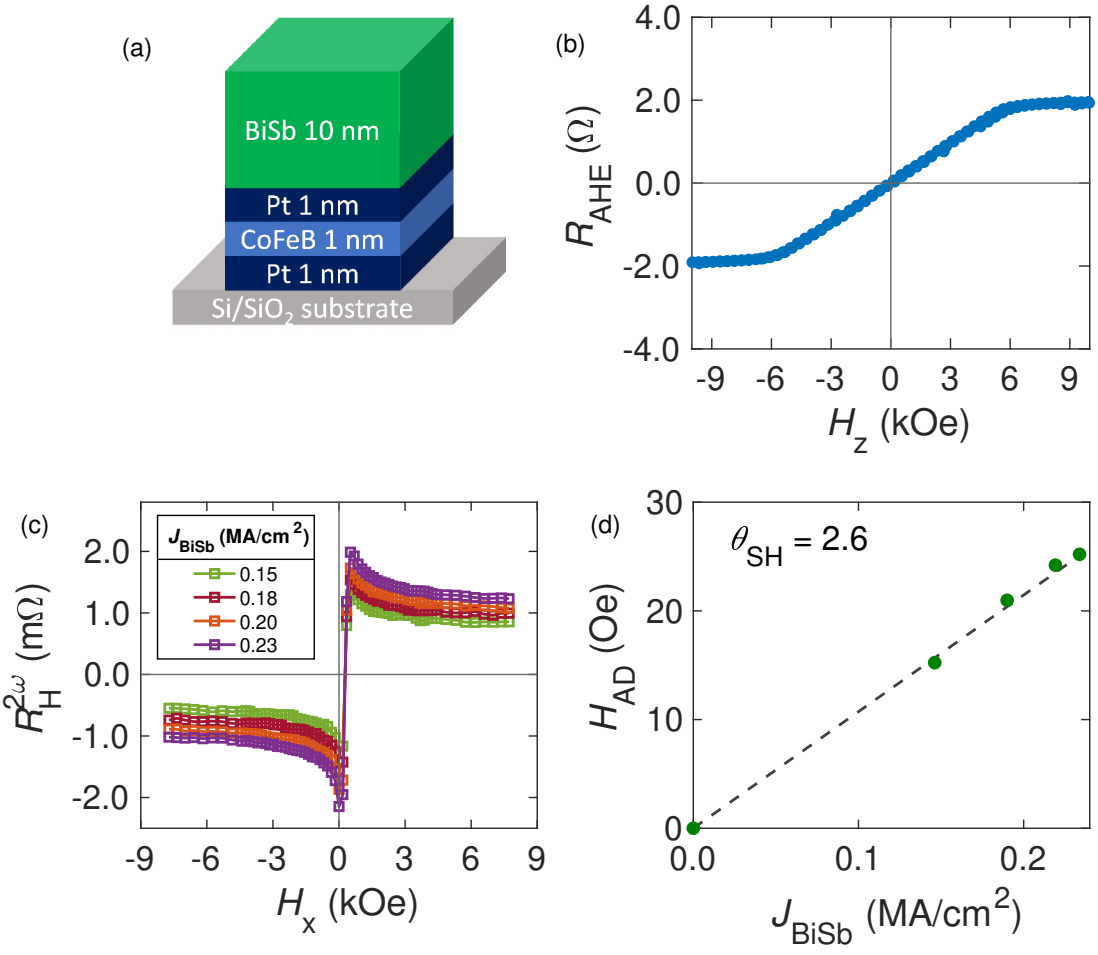

Figure 4.4: Stack A. (a) Schematic structure. (b) Anomalous Hall resistance. (c) Second harmonic Hall resistance at $J_{\mathrm{BiSb}} = 0.15,\ 0.18,\ 0.20,$ and $0.23\,\mathrm{MA/cm^2}$. (d) Extracted antidamping-like field H_{AD} as a function of J_{BiSb}.

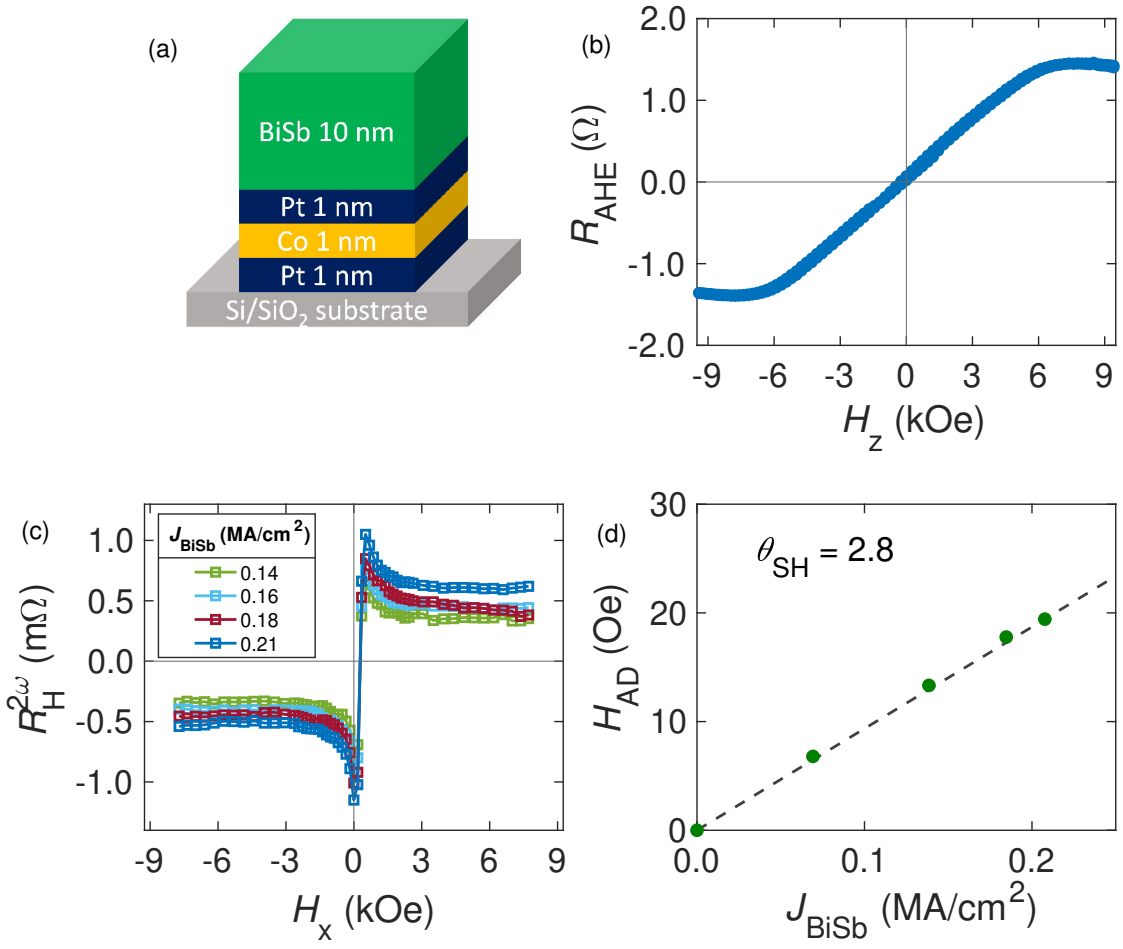

Figure 4.5: Stack B. (a) Schematic structure. (b) Anomalous Hall resistance. (c) Second harmonic Hall resistance at $J_{\mathrm{BiSb}} = 0.14,\ 0.16,\ 0.18,$ and $0.21\,\mathrm{MA/cm^2}$. (d) Extracted antidamping-like field H_{AD} as a function of J_{BiSb}.

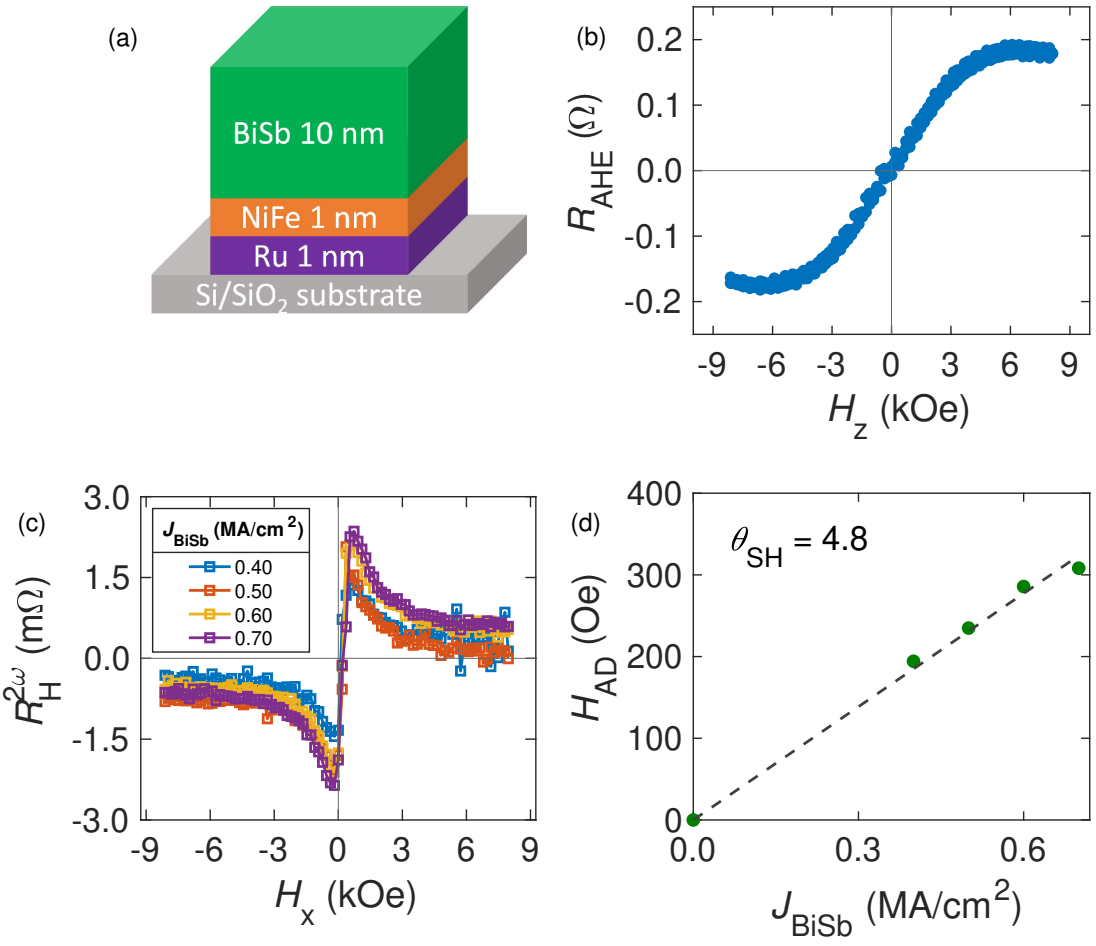

Figure 4.6: Stack C. (a) Schematic structure. (b) Anomalous Hall resistance. (c) Second harmonic Hall resistance at 0.40, 0.50, 0.60, and 0.70 MA/cm^2. (d) Extracted antidamping-like field H_{AD} as a function of J_{BiSb}.

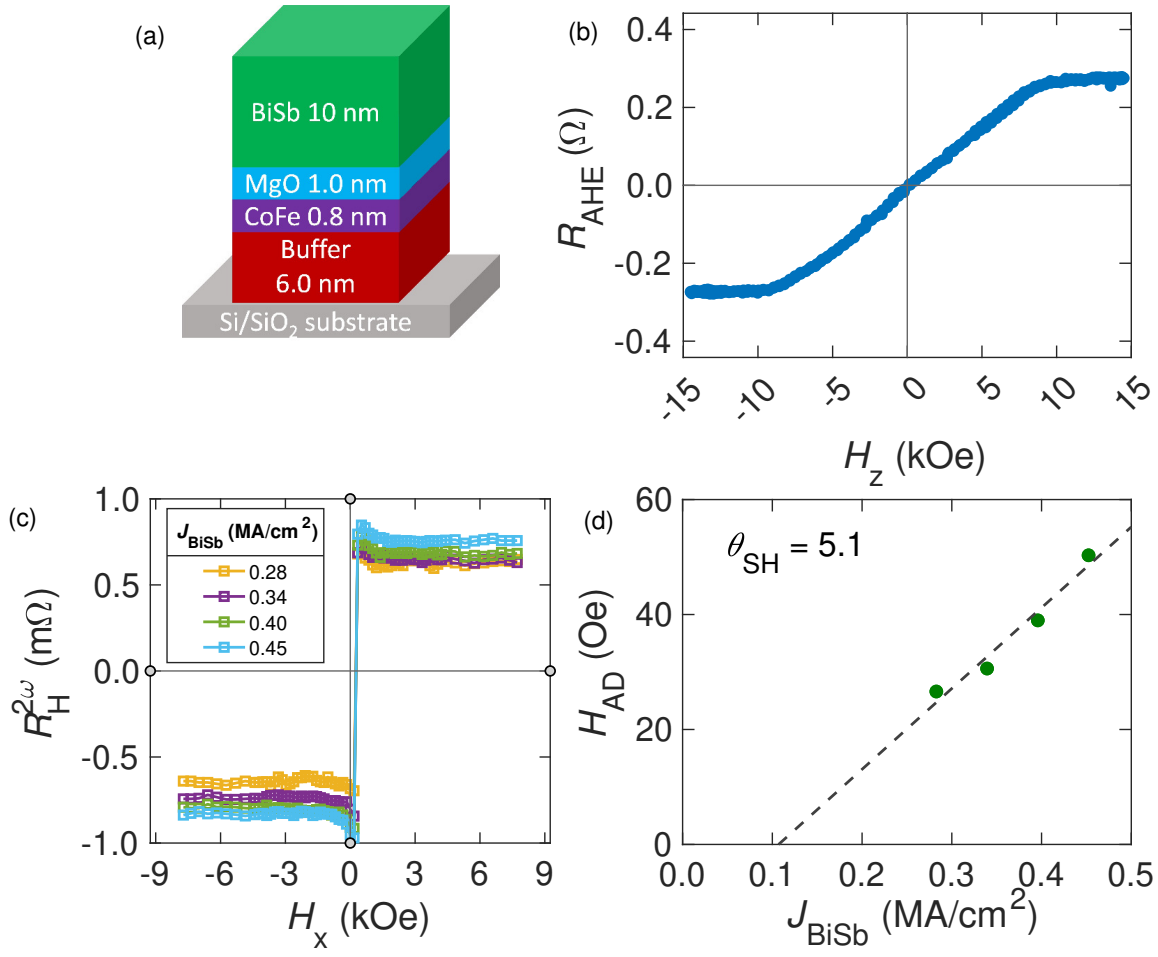

Figure 4.7: Stack D. (a) Schematic structure. (b) Anomalous Hall resistance. (c) Second harmonic Hall resistance at $J_{\mathrm{BiSb}} = 0.28,\ 0.34,\ 0.40,$ and $0.45\,\mathrm{MA/cm^2}$. (d) Extracted antidamping-like field H_{AD} as a function of J_{BiSb}.

4.4 Large inverse spin Hall effect in BiSb topological insulator for 4 Tb/in^2 magnetic recording technology

In this section, we demonstrate a proof-of-concept of the SOT reader with a significantly enhanced output voltage by integrating BiSb with large spin Hall angle.

4.4.1 Proof-of-concept BiSb-based SOT reader

In the previous works on sputtered BiSb, an impressive θ_{SH} has been reported in BiSb on top of FM layers [11, 12, 13, 14, 15] than that in FM on top of BiSb [30]. This is resulted from the unusual large grain size and the large surface roughness of BiSb compared with the thickness of the FM layers [31]. Therefore, here we use the previously optimized CoFe/MgO/BiSb (top) stack in the proof-of-concept SOT reader. Moreover, we particularly chose CoFe because of its high spin polarization P. The interfacial layer of MgO is used to further fuel the spin polarization thanks to the spin-filtering effect [27, 28, 29] and protect the CoFe layer from damage by Sb diffusion during BiSb sputtering.

4.4.1.1 Device fabrication process

To begin with, we introduce the process consisting of six cycles of optical lithography and lift-off to fabricate the SOT reader as shown in Figure 4.8. In the first step, we prepare a bottom electrode I_- made of Ta (15 nm)/Pt (5 nm). Next, the main pillar, from top to bottom, consisting of a Pt (1 nm)/BiSb (10 nm)/MgO (2 nm)/CoFe (5 nm) is deposited on the bottom electrode. The Pt layer works as a capping layer to prevent possible damage to the BiSb layer from wet process and air exposure. The area size of the pillar is 20 μm × 20 μm. Afterwards, an insulator of MgO (18 nm)/NiO (2 nm) is deposited to avoid shunting between the top and bottom electrodes. Then, Ta (15 nm)/Pt (5 nm) electrodes sequentially sputtered as voltage leads V_+ and V_-. To eliminate any possible in-plane shunting, a notch

is designed to force the current to flow vertically from the top electrode through the main pillar. To do so, a barrier made by MgO (18 nm)/NiO (2 nm) is deposited on top and the notch is opened in the fifth lift-off. Finally, Ta (45 nm)/Pt (15 nm) layers as top electrode I_+ is deposited on top of the notch for electrical contact with the main pillar. Figure 4.9 (a) shows a schematic structure of fabricated SOT reader and Figure 4.9 (b) shows a top-view optical image of a completed SOT reader and the experimental setup to measure the ISHE. We applied a perpendicular bias charge current to the pillar via a current injection window with the size of 8 µm × 20 µm, and measured the output voltage V_{ISH} between V_+ and V_- while sweeping H_{x}.

4.4.1.2 Inverse spin Hall resistance in device A

Figure 4.10 (a) shows a representative inverse Hall resistance $R_{\mathrm{ISH}} = V_{\mathrm{ISH}}/I$ as a function of H_{x} in device A, measured with $J = 31$ kA/cm^2 at room temperature. We observe a large R_{ISH} of 0.11 Ω. By measuring the resistance between the V_+ and V_- leads, we found a $R_{\mathrm{sheet}}^{\mathrm{BiSb}} = 785\,\Omega$ in this device. Substituting this $R_{\mathrm{sheet}}^{\mathrm{BiSb}}$ and the device width $w_{\mathrm{BiSb}} = 20$ µm to Equation (4.2), we obtained $\theta_{\mathrm{SH}} = 6.1$ for BiSb in device A. This value is close to $\theta_{\mathrm{SH}} = 5.1$ for the SHE measured by the second harmonic Hall resistance technique in sample D in Section 4.3. Figure 4.10 (b) shows the output voltage V_{ISH} – J characteristic of device A. The output voltage is about few mV, which is at least four orders of magnitude larger than that observed in Pt/CoFe junctions ($V_{\mathrm{ISH}} = 75$ nV at 100 kA/cm^2 for a 260 nm device at 10 K mentioned in the Supplementary Figure 6 of Reference [5]. This large output voltage cannot be induced by either anomalous Nernst effect (ANE) or AHE of CoFe. Indeed, the linearity observed in Figure 4.10 (b) denies the contribution of ANE of CoFe while the R_{AHE} of CoFe in this 20 µm wide device with the perpendicular bias current is approximately 2 mΩ. Hence, this large output R_{ISH} of 0.11 Ω is the manifestation of the large ISHE from BiSb.

4.4.1.3 Inverse spin Hall resistance in device B

Figure 4.11 (a) shows the R_{ISH} as a function of H_{x} in device B biased by $J = 6.3\,\mathrm{kA/cm^2}$ at room temperature. The R_{ISH} is as large as 1.1 Ω. Figure 4.11 (b) shows the $V_{\mathrm{ISH}} - J$ characteristic of device B. Noticeably, V_{ISH} reaches 15 mV at $J = 9.4\,\mathrm{kA/cm^2}$. From this large signal, we expect a giant $\theta_{\mathrm{SH}} = 61$ in device B. This value is close to $\theta_{\mathrm{SH}} = 52$ originally reported in MnGa/BiSb(012) epitaxially grown by MBE. Thanks to this giant θ_{SH}, a very low bias current of only 13.5 μA or 3.38×10^6 A/cm^2 is feasible in a 20 nm × 20 nm SOT reader. This also provides a substantial margin for further device scaling, allowing for advancements beyond 4 Tb/in^2 in magnetic recording technology.

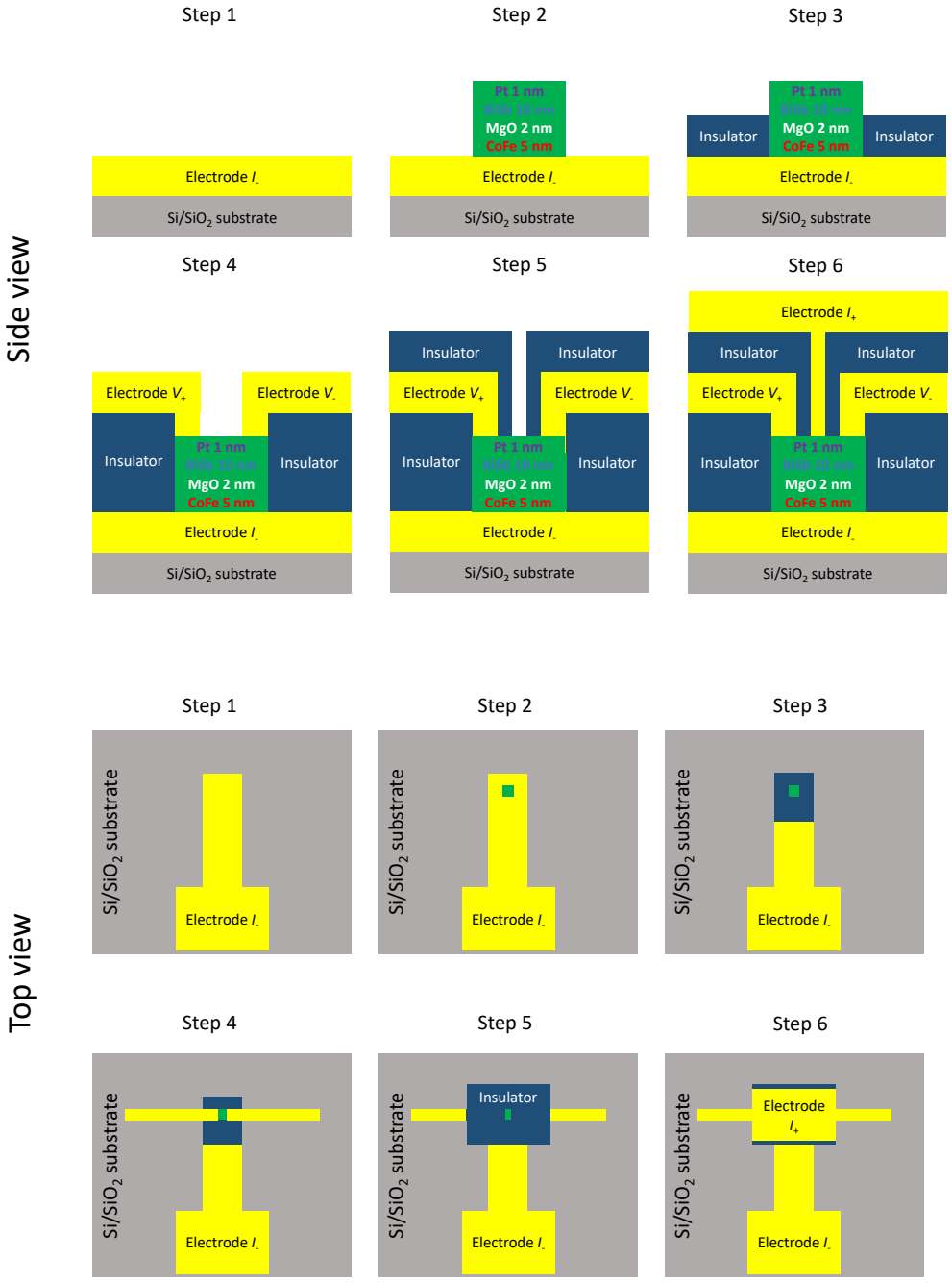

Figure 4.8: A completed fabrication process of the SOT reader from a side view (top) and a top view (bottom).

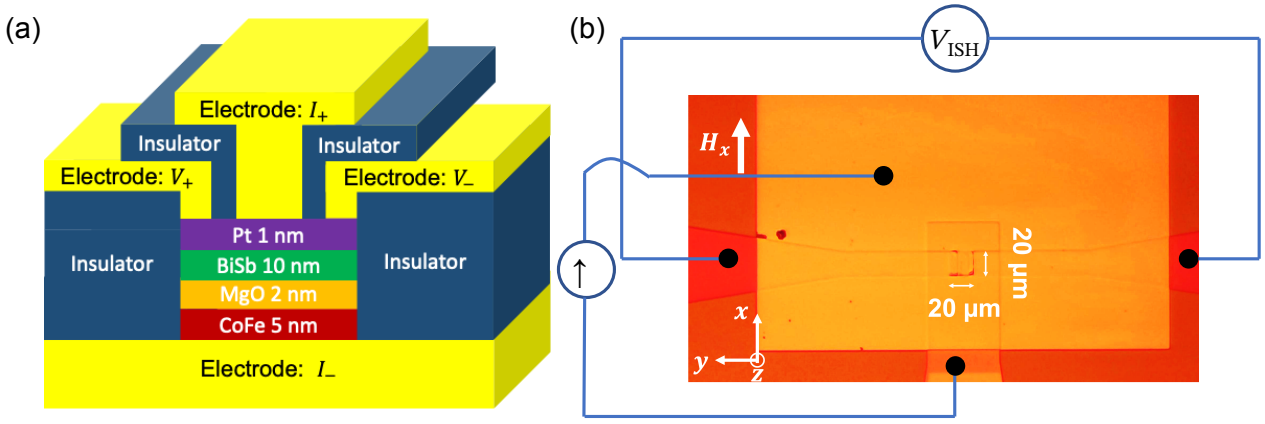

Figure 4.9: (a) Schematic structure of fabricated SOT readers. (b) Top view optical image and experiment set up of a 20 μm × 20 μm device.

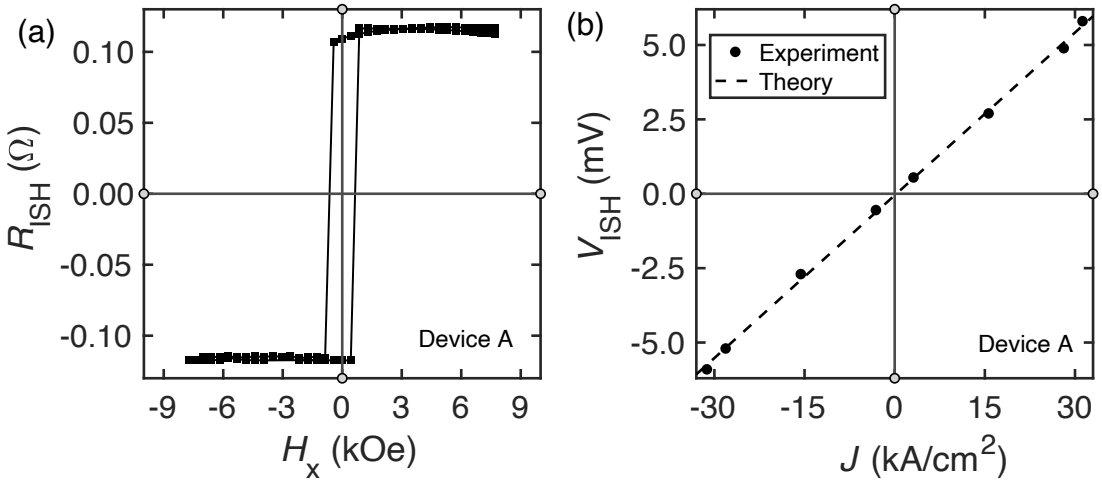

Figure 4.10: (a) Inverse spin Hall resistance R_{ISH} curve of device A, measured with a bias current density $J = 31\,\mathrm{kA/cm^2}$. (b) $V_{\mathrm{ISH}} - J$ characteristic of device A.

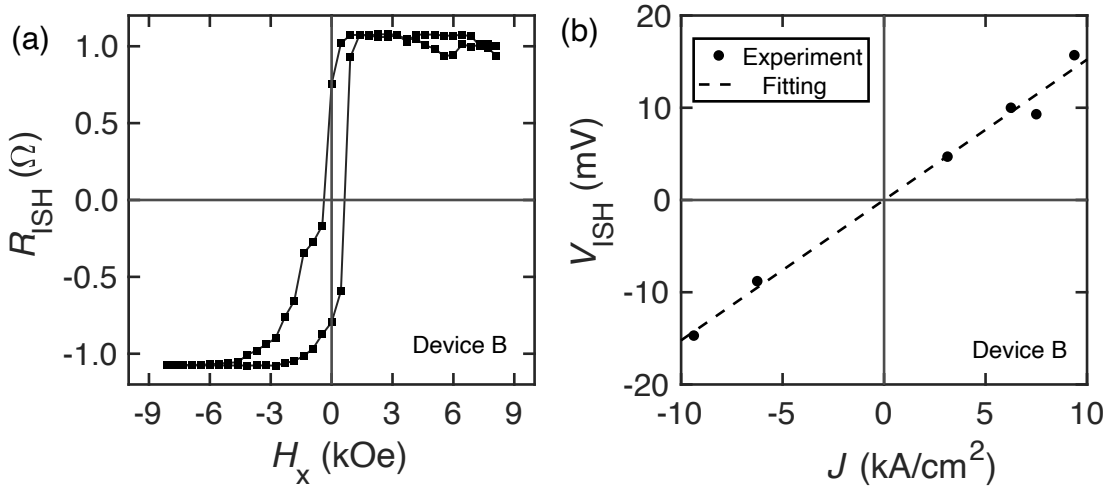

Figure 4.11: (a) Inverse spin Hall resistance R_{ISH} curve of device B, measured with a bias current density $J = 6.3\,\mathrm{kA/cm^2}$. (b) $V_{\mathrm{ISH}} - J$ characteristic of device B.

4.5 Discussion

4.5.1 The difference between device A and B performance

The large difference in θ_{SH} between device A and B can be attributed to the intrinsic spin Hall effect's dependence on the number of Dirac cones present in the topological surface states, which varies with the crystal orientation of BiSb. For instance, the BiSb (012) topological surface features four Dirac cones located at the $\bar{\Gamma}$, $\bar{X}_1$, $\bar{M}$, and near the $\bar{X}_2$ points [32]. Since Dirac cones act as monopoles of Berry phase [33], the BiSb (012) surface exhibits the largest spin Hall angle through the intrinsic mechanism. In contrast, the BiSb (001) surface has only one Dirac cone at the Γ point [34], resulting in a smaller spin Hall angle. Indeed, previous studies have demonstrated a large θ_{SH} of 52 for epitaxial BiSb (012) [11], θ_{SH} of 10.7 for highly textured BiSb (110) [14], and a much smaller θ_{SH} of 3.2 for highly textured BiSb (001) [12]. Therefore, the observed θ_{SH} in this work likely depends on the crystal orientation of BiSb, which is influenced by the crystallinity of the underlying MgO and CoFe layers. If the MgO and CoFe layers exhibit a well-textured cubic (001) orientation, pseudo-cubic BiSb (012) will preferentially grow, which may explain the larger θ_{SH} in device B. Conversely, if the MgO and CoFe layers are polycrystalline, the resulting BiSb layer will also be polycrystalline, as seen in device A with the smaller θ_{SH}. Thus, achieving BiSb (012) with a high θ_{SH} requires growing highly textured CoFe (001) and MgO (001). This, in turn, requires a suitable buffer or electrode material beneath the CoFe layer that promotes their (001) orientations.

In this work, we utilized the lift-off process to deposit the sensor pillar on top of the bottom electrode, selecting Ta/Pt as the bottom electrode to avoid oxidation during air exposure and wet processing. However, the Ta/Pt bottom electrode is not optimized for the growth of highly textured CoFe (001)/MgO (001)/BiSb (012), leading to variations in the θ_{SH} of the resulting SOT readers. In practical sensor fabrication, etching techniques like ion milling can be employed instead of the lift-off process to fabricate SOT sensors. This would allow the use of a different buffer/electrode material that promotes the growth of highly textured CoFe (001)/MgO (001)/BiSb (012), resulting in SOT sensors with consistently large

θ_{SH} and high yield.

Alternatively, BiSb could be deposited first on top of the bottom electrode, followed by MgO/CoFe on top of BiSb, with a buffer/electrode material that encourages the BiSb(012) crystal orientation. Recent work has demonstrated the growth of highly textured BiSb with either strong (001) or strong (012) crystal orientations by selecting appropriate buffer layers [31]. In this study, we observed that the grain size of 10 nm thick BiSb is approximately 40 nm. In the ideal case of epitaxial BiSb, there are no grain boundaries. Therefore, a 20 nm sensor device would either be positioned on a single grain or, at worst, on a single grain boundary, which would not adversely affect device performance as long as the crystal orientation of the BiSb grains remains consistent.

4.5.2 The difference between spin Hall angle measured by different techniques

Here we provide the explanation for the larger θ_{SH} of BiSb in CoFe/MgO/BiSb stack observed by the ISH comparing with that obtained by the second harmonic Hall technique in Section 4.3. In the second harmonic Hall measurement, an alternating pure spin current is generated via the SHE when an in-plane AC current is applied to BiSb. The pure spin current diffuses into the FM layer and exerts a spin-orbit torque on it. The oscillation of the magnetization of the FM layer caused by the SOT produces a second harmonic Hall resistance. The amplitude of the second harmonic Hall resistance for a system with IMA is governed by Equation 4.7. Given that H_{AD} is approximately 10 Oe for CoFe, it is crucial to minimize H_k to several kOe to achieve a significant $R_H^{2\omega}$. Takning into account that the bulk shape magnetic anisotropy of CoFe is 18.8 kOe, it is necessary to reduce the thickness of CoFe to 0.9 nm. This engineering helps enable the interfacial PMA between MgO and CoFe to compete with the bulk shape anisotropy. Indeed, we observed a reduction of H_k to 9 kOe. Unfortunately, CoFe is more susceptible to Sb diffusion from BiSb when its thickness is extremely thin. Moreover, the MgO layer is recognized for its ability to impede the diffusion of pure spin currents. Consequently, the θ_{SH} obtained by the second harmonic Hall approach

represents an effective value that is less than the intrinsic value. In the SOT reader, there is only a spin-polarized charge current injected from CoFe to BiSb. The 5 nm CoFe layer may be sufficiently thick to withstand Sb diffusion. Additionally, the 2 nm thick MgO layer may be helpful to partially block Sb diffusion while enhancing spin polarization through its spin filtering effect. As a result, the θ_{SH} obtained via the inverse spin Hall effect approximates the intrinsic value.

4.6 Conclusion

In conclusion, we conducted a noise analysis to determine the relationships between SNR and θ_{SH} in 20 nm $\times$ 20 nm BiSb-based SOT readers. We established a minimum θ_{SH} of 2 to achieve an SNR of 28 dB at a bias current of 400 µA. We subsequently demonstrated proof-of-concept BiSb-based SOT reader, achieving large output voltages of up to 15 mV at a bias current density of 9.4 $\mathrm{kA/cm^2}$ at room temperature, from which we project a giant $\theta_{\mathrm{SH}} = 61$. Our findings demonstrate the capability of BiSb for SOT readers beyond 4 $\mathrm{Tb/in^2}$ in magnetic recording technology. Finally, the findings of this study can also be employed as the spin-orbit module in the output stage of magnetoelectric spin–orbit logic devices, which have been recently suggested as an alternative to Si transistors for low power computing [35].

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Chapter 5: Integration of BiSb topological insulator and CoFeB/MgO with perpendicular magnetic anisotropy using an oxide interfacial layer for ultralow power SOT-MRAM cache memory

Besides the application in SOT readers, which targets the bottom of the memory hierarchy, BiSb as the spin current injector, can also contribute to realizing ultrafast SOT-MRAM, which is forecasted to replace SRAM as cache memory in the top levels. However, the large spin Hall angles have been reported so far only in BiSb deposited on top of Co/Pt and Co/Tb multilayers. In a realistic SOT-MRAM application, it is essential to integrate BiSb to CoFeB/MgO junction with PMA. In this chapter, we report a large spin Hall angle of 2.8 in junctions of bottom BiSb and CoFeB/MgO with PMA using a CrO_x interfacial layer, which is suitable for use in the MTJ. We demonstrated SOT magnetization switching by a small current density of 3.1 MA/cm^2 with a pulse width of 50 µs, which is an order of magnitude smaller than that in HMs. Our work demonstrates the capability of integrating BiSb to CoFeB/MgO-based MTJ with possible applications in cache memories.

5.1 Introduction

SOT-MRAM comprises a spin current injector for writing and an MTJ for reading. Thanks to its outstanding read/write speed and extended device lifetime [1], SOT-MRAM

is favorable to serve as embedded memories. The works on SOT-MRAM are centered on the search for a spin current injector with a large spin Hall angle. So far, HMs have been rigorously studied for this functionality [2, 3, 4]. However, HMs are associated with small spin Hall angles such as $\theta_{SH} = 0.15$ for Ta [2] and 0.4 for W [4], which demands high energy to write the data, especially in the perpendicular-MTJ (p-MTJ). In this regard, TI, a quantum material with strong SHE, is a promising candidate. TI possesses semiconducting bulk states and Dirac-like two-dimensional conductive surface states [5, 6, 7]. TIs have a spin-momentum locking characteristic in their surface states [8] due to large SOC and a topological band structure, enabling the generation of pure spin currents in a direction orthogonal to the film plane [9]. Numerous studies have shown TIs exhibiting a superior spin Hall angle, including Bi_2Se_3 [10] and $(BiSb)_2Te_3$ [11], grown by MBE. Nevertheless, the electrical conductivity of these TIs ($\sigma \approx 10^4\,\Omega^{-1}\mathrm{m}^{-1}$) is typically one or two orders of magnitude lower than that of metallic FMs. As a result, there is a large shunting current which reduces the high performance of SOT-MRAM. Recently, the alloy $Bi_{1-x}Sb_x$ ($0.07 \leq x \leq 0.22$) has shown itself as an attractive TI with a colossal spin Hall angle $\theta_{SH} \approx 52$ and high electrical conductivity $\sigma_{BiSb} = 2.5 \times 10^5\,\Omega^{-1}\mathrm{m}^{-1}$ in junction with MnGa fabricated by MBE [12]. Since then, many works have been conducted to achieve relatively large θ_{SH} ($1.2 \sim 10.7$) and sufficiently high σ_{BiSb} ($1.1 \sim 1.8 \times 10^5\ \Omega^{-1}\mathrm{m}^{-1}$) in BiSb deposited by industry-friendly magnetron sputter [13, 14, 15, 16, 17]. These reports successfully achieved large spin Hall angles of sputtered BiSb on top of ferrimagnetic Co/Tb [13] or FM Co/Pt multilayers [14, 15, 16], owing to a smooth interface and minimal intermixing between them. In realistic SOT-MRAM applications, CoFeB/MgO-based p-MTJ is well-known for its high TMR [18]. Therefore, it is necessary to integrate BiSb with large θ_{SH} and σ_{BiSb} to CoFeB/MgO junction with PMA. To realize PMA in CoFeB/MgO, post annealing process is necessary to crystallize CoFeB to bcc-CoFe and to induce an interfacial PMA between CoFeB and MgO [19]. However, there is concern that a post-annealing process may exacerbate the Sb diffusion which damages the CoFeB and degrades PMA. In this chapter, we focused on developing an oxide interfacial layer in between BiSb and CoFeB/MgO to achieve PMA together with a large spin Hall angle. The use of the oxide interface can bring three benefits:

1. An oxide layer can play the role of barrier to protect CoFeB from Sb diffusion which may damage the CoFeB/MgO junction and deteriorate PMA. Furthermore, this diffusion barrier also help protect BiSb TSSs. Thus, a large θ_{SH} can be preserved via the intrinsic mechanism mentioned in Chapter 2.

2. An oxide layer can reduce unfavorable shunting charge current flowing into the FM layer thanks to its high resistivity while it still allows spin current to be injected through because of its spin transparency. Indeed, inserting NiO between BiSb bottom and Co can help improve θ_{SH} of sputtered BiSb up to 10.3 [20]. This enhancement is possible thanks to the long spin diffusion length of NiO that increases θ_{SH} via the extrinsic mechanism.

3. For BiSb-on-top-of-MTJ structure, the MTJ pillar is sputtered first following by sputtered BiSb. In this case, an oxide layer can also serve as a protection layer of the underneath FM layers.

Hence, it is necessary to find an oxide interfacial layer that can suppress Sb diffusion but still allows spin diffusion to obtain PMA and a large spin Hall angle in BiSb-integrated CoFeB/MgO-based MTJ.

5.2 NiO as interfacial layer

Following the success of BiSb(bottom)/NiO (1 $\sim$ 3 nm)/Co [20], first we preliminarily investigate the possibility of NiO as the interfacial layer between the BiSb bottom and CoFeB/MgO junction. First, we sequentially deposited BiSb (10.0 nm)/NiO (1.0 $\sim$ 3.0 nm)/Ta (0.8 nm)/$Co_{20}Fe_{60}B_{20}$ (0.9 nm)/MgO (2.0 nm)/Ta (2.0 nm) on c-plane sapphire substrates by magnetron sputtering at room temperature. The NiO layers in these stacks were deposited by RF sputtered from a ceramic NiO single target. The stack was then post-growth annealed at 250°C for one hour. Unfortunately, for 1 nm thick NiO, we could not achieve PMA of Ta/CoFeB/MgO. In the case of thicker NiO from 2 – 3 nm, the PMA could be achieved but the spin Hall angles were only 0.4 – 0.7 as summarized in Figure 5.1.

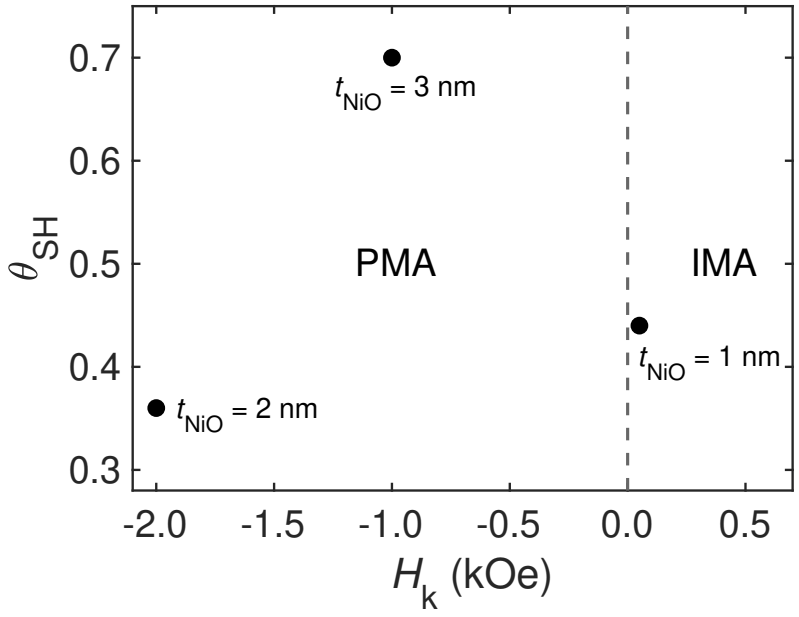

Figure 5.1: Summary of the anisotropy effective field and spin Hall angle of BiSb (10.0 nm)/NiO (1.0 $\sim$ 3.0 nm)/Ta (0.8 nm)/$Co_{20}Fe_{60}B_{20}$ (0.9 nm)/MgO (2.0 nm)/Ta (2.0 nm).

This performance can be attributed to two possible factors. First, crystallized NiO has large surface roughness. At the thin NiO case, the roughness may degrade the interfacial PMA between CoFeB and MgO. Second, large θ_{SH} of BiSb have been reported so far only when NiO is adjacent to the FM layer, as in the case of BiSb/NiO/Co. In the case of BiSb integration with CoFeB/MgO, an additional Ta is inserted between NiO and CoFeB to absorb B during post annealing for the crystallization of CoFeB and achieving PMA. Thus, without the direct contact with CoFeB, small θ_{SH} was observed in this set of samples.

The failure of NiO suggests that amorphous oxide layer may be a solution to achieve PMA while maintaining large spin Hall angle in the stack of BiSb/oxide interface/Ta/CoFeB/MgO. In the next section, we adopted amorphous CrO_x as the oxide interfacial layer in between BiSb and the Ta/CoFeB/MgO trilayers

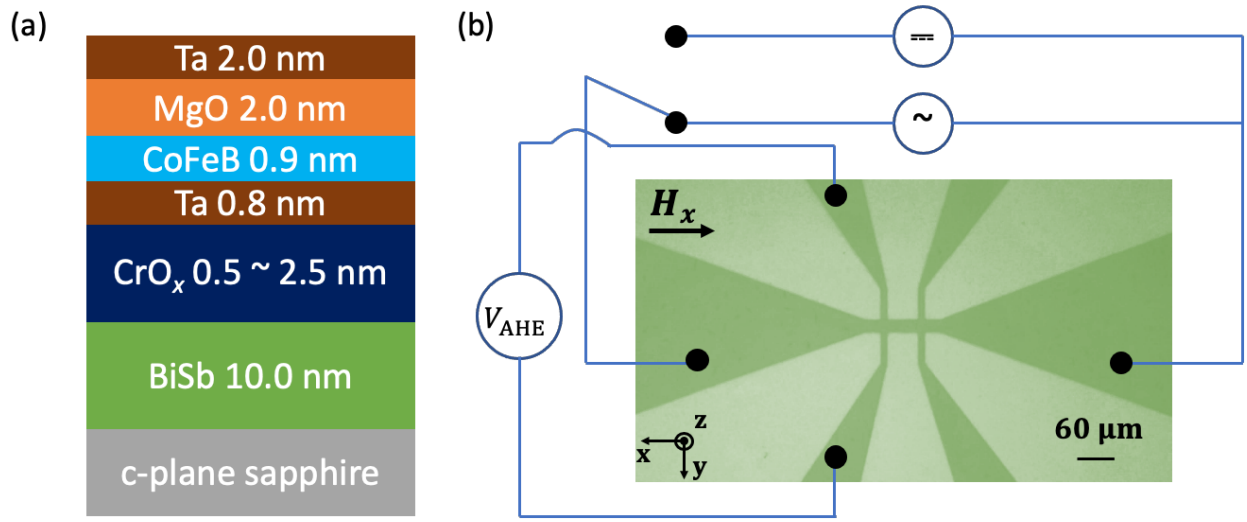

Figure 5.2: (a) Schematic structure of our samples. (b) Optical image and experimental set up for spin Hall angle evaluation.

5.3 CrO_x as interfacial layer

In this section, we sequentially fabricated a series of BiSb (10.0 nm)/CrO_x (0.5 $\sim$ 2.5 nm)/Ta (0.8 nm)/$Co_{20}Fe_{60}B_{20}$ (0.9 nm)/MgO (2.0 nm)/Ta (2.0 nm) on c-plane sapphires substrate by magnetron sputtering at room temperature as schematically shown in Figure 5.2 (a). Here, the CrO_x was reactively sputtered with oxygen from a Cr single target. Afterwards, the stacks were undergone a post annealing at 250°C for one hour. During the annealing, CoFeB was crystallized to bcc-$Co_{25}Fe_{75}$ with high saturation magnetization $M_s = 1800$ emu/cm^3, which was later confirmed by SQUID meaasurement.

Finally, we patterned 20 $\times$ 60 μm^2 six-terminal Hall bar devices of these stacks using optical lithography. Figure 5.2 (b) shows an optical image of a Hall bar device and the measurement configuration for θ_{SH} measurement. Our experiment is conducted as follows. First, we measured the anomalous Hall resistance R_{AHE} with a small DC under H_z and H_x, respectively. Next, we adopted the second harmonic Hall resistance measurement [21] to evaluate the spin Hall effect. To do so, we injected an 259.68–Hz AC to the Hall bar and probed the first and second harmonic Hall voltages V_H^{ω}, $V_H^{2\omega}$ using a lock-in amplifier while

scanning H_{x} . Under the SOT magnetic field, $R_{\mathrm{H}}^{2\omega}$ was modulated by the oscillation of the net magnetic moment. Eventually, we extracted the antidamping-like field H_{AD} by fitting the second harmonic Hall resistance signal using the following equation:

$$R_{\mathrm{H}}^{2\omega} = \frac{R_{\mathrm{AHE}}}{2}\frac{H_{\mathrm{AD}}}{H_{\mathrm{x}} - H_{\mathrm{k}}} + R_{\mathrm{ONE}}H_{\mathrm{x}} + R_{\mathrm{ANE+SSE}}. \tag{5.1}$$

To obtain H_{k}, we fitted the $R_{\mathrm{AHE}} - H_{\mathrm{x}}$ data obtained from V_{H}^{ω} using the following equation:

$$R_{\mathrm{AHE}} = R_{\mathrm{AHE}}(0)\sqrt{1 - \left(\frac{H_{\mathrm{x}}}{H_{\mathrm{k}}}\right)^2}, \tag{5.2}$$

where $R_{\mathrm{AHE}}(0)$ is the anomalous Hall resistance at $H_{\mathrm{z}} = 0$ kOe. Finally, the spin Hall angle θ_{SH} is calculated from:

$$\theta_{\mathrm{SH}} = \frac{2e}{\hbar}t_{\mathrm{CoFeB}}M_{\mathrm{s}}\frac{\partial H_{\mathrm{AD}}}{\partial J_{\mathrm{BiSb}}}. \tag{5.3}$$

5.3.1 Dependence of PMA and SOT characteristics on CrO_x thickness

In this part, we examine the SOT characteristics of the film stacks of $Bi_{90}Sb_{10}$ (10 nm)/CrO_x (0.5 $\sim$ 2.5 nm, changed by 0.5 nm step)/Ta (0.8 nm)/$Co_{20}Fe_{60}B_{20}$ (0.9 nm)/MgO (2.0 nm)/Ta (2.0 nm) sputtered on c-plane sapphire substrate. We designated these samples as A-1 (t_{CrO_x} = 0.5 nm) through A-5 (t_{CrO_x} = 2.5 nm). Here we note that $Bi_{90}Sb_{10}$ was sputtered using a single target in this set of samples. For further estimation, we sputtered a stand-alone 10 nm $Bi_{90}Sb_{10}$ thin film to measure the electrical conductivity which yields $\sigma_{\mathrm{BiSb}} = 1.8 \times 10^5\,\Omega^{-1}\mathrm{m}^{-1}$. This result agrees with previous report of sputtered BiSb on c-plane sapphire [22].

First, we show the magnetic characteristics and θ_{SH} of two representative samples A-2 (t_{CrO_x} = 1.0 nm) and A-5 (t_{CrO_x} = 2.5 nm). The R_{AHE} of sample A-2 as a function of H_{z} and H_{x} are displayed in Figure 5.3 (a) and (b), respectively. With $R_{\mathrm{AHE}} = 2.2\,\Omega$ and $H_{\mathrm{k}} = 1.4\,\mathrm{kOe}$, we confirmed a distinct PMA in sample A-2 with 1 nm thick CrO_x. Then, Figure 5.3 (c) shows $R_{\mathrm{H}}^{2\omega}$ as a function of H_{x} induced by various current densities $J_{\mathrm{BiSb}} = 0.69,\ 0.79,\ 0.90,\ 1.00\,\mathrm{MA/cm}^2$. Finally, 5.3 (d) shows the $H_{\mathrm{AD}} - J_{\mathrm{BiSb}}$ relationships

extracted from Figure 5.3 (c). With 62% of the applied current density flowing in the BiSb layer under parallel conduction model, we achieved an effective θ_{SH} of 2.5. To verify the parasitic SOT effect from the 0.8 nm thin Ta in this stack, we prepared a reference sample of Ta (0.8 nm)/$Co_{20}Fe_{60}B_{20}$ (0.9 nm)/MgO (2.0 nm)/Ta (2.0 nm) under same fabrication condition and confirmed a tiny θ_{SH} of 0.02 which can be neglected.

Next, we evaluate the sample A-5 with a thicker CrO_x interface of 2.5 nm. Figure 5.4 (a) and (b) show R_{AHE} of the sample A-5 as a function of H_{z} and H_{x}, respectively. We observed a slight increment in R_{AHE} up to $2.7\,\Omega$ and a significantly stronger $H_{\mathrm{k}} = 4.6\,\mathrm{kOe}$, which is nearly three times greater than that in sample A-2. These results suggest that increasing the thickness of the CrO_x interfacial layer can enhance the PMA, which indicates that the CrO_x interfacial layer indeed successfully suppressed Sb diffusion to the CoFeB layer during post annealing at 250°C and protect the interfacial PMA between CoFeB and MgO layers. Figure 5.4 (c) shows $R_{\mathrm{H}}^{2\omega}$ as a function of H_{x} induced by several current densities $J_{\mathrm{BiSb}} = 0.74, 0.86, 0.97, 1.09\,\mathrm{MA/cm^2}$. Finally, from the extracted $H_{\mathrm{AD}} - J_{\mathrm{BiSb}}$ relationships shown in Figure 5.4 (d), we observed an effective θ_{SH} of 1.2, which is approximately half of the value measured in sample A-2. The smaller effective θ_{SH} of sample A-5 can be accounted for the smaller spin transparency of the thicker CrO_x interfacial layer.

To summarize this section, we show the H_{k} and θ_{SH} of samples A1–A5, as functions of the CrO_x interfacial layer thickness $t_{\mathrm{CrO}_x} = 0.5 \sim 2.5$ nm in Figure 5.5 (a) and (b), respectively. There is a clear trade-off between H_{k} and θ_{SH}. As shown in Figure 5.5 (a), H_{k} is lowest at $t_{\mathrm{CrO}_x} = 1\,\mathrm{nm}$ and gradually increases for $1\,\mathrm{nm} < t_{\mathrm{CrO}_x} \leq 2.5\,\mathrm{nm}$. In contrast, θ_{SH} reaches its maximum value of 2.5 at $t_{\mathrm{CrO}_x} = 1\,\mathrm{nm}$ and steadily decreases as t_{CrO_x} increases within the range of $1\,\mathrm{nm} < t_{\mathrm{CrO}_x} \leq 2.5\,\mathrm{nm}$. The enhancement of spin Hall angle by inserting CrO_x layer can be explained via the intrinsic and extrinsic mechanism using Equation (2.21) and (2.22) in Chapter 2. In case of BiSb TI with a thin spin-momentum locking surface state, one can rewrite the charge-to-spin conversion as:

$$\theta_{\mathrm{SH}} = T_{\mathrm{int}} \theta_{\mathrm{SH}}^{\mathrm{intr}}, \tag{5.4}$$

where T_{int} is the interfacial spin transparency that satisfies

$$T_{\text{int}} \propto \frac{1}{v_{\text{F}}(\tau_{\text{t}} + \tau_{\text{mix}})}. \tag{5.5}$$

When Sb diffusion happens, the TSSs of BiSb is degraded, which results in smaller intrinsic $\theta_{\text{SH}}^{\text{intr}}$ and consequently a small effective spin Hall angle θ_{SH}. As increasing the CrO_x thickness, the thick CrO_x suppresses the Sb diffusion to protect the TSSs of BiSb. Thus, the CrO_x can prevent the degradation of intrinsic $\theta_{\text{SH}}^{\text{intr}}$. These factors are responsible for the strong SHE at $t_{CrO_x} = 1$ nm. However, because of the thick interfacial layer, the denominator in Equation (5.5) significantly increases which reduces the spin transparency. In the case of $t_{CrO_x} = 1$ nm, it may be sufficient to partially suppress Sb diffusion while facilitating a good spin transparency. Hence, such a condition is favorable to achieve $\theta_{\text{SH}} = 2.5$ together with a PMA. However, when $t_{CrO_x} > 1$ nm, the spin transparency is reduced, resulting in smaller θ_{SH}.

Regarding the cache memory application, on one hand, with low H_{k} and large θ_{SH}, the sample A-2 promises to serve in ultra-fast and short-term memory applications such as high-level cache memory, where ultra-fast writing speed is prioritized. On the other hand, the sample A-5 with high H_{k} but smaller θ_{SH} is more suitable for storage-like long-term memory applications, where data lifetime is emphasized and longer writing latency is acceptable. Further discussion on retention time will be provided at the end of this chapter.

5.3.2 SOT magnetization switching in sample B

Following the study on the dependence of PMA characteristics and spin Hall angle on the thickness of CrO_x interfacial layer, in this section, we demonstrate type-z SOT magnetization switching in a sample B with the structure of $Bi_{85}Sb_{15}$ (10.0 nm)/CrO_x (1.0 nm)/Ta (0.8 nm)/CoFeB (1.0 nm)/MgO (2.0 nm)/Ta (2.0 nm) shown in Figure 5.6 (a). Here we noted that the $Bi_{85}Sb_{15}$ layer in sample B was co-sputtered of Bi and Sb targets which yields a lower $\sigma_{\text{BiSb}} = 1.3 \times 10^5\,\Omega^{-1}\text{m}^{-1}$ in a 10 nm stand-alone $Bi_{85}Sb_{15}$. This is slightly lower than that of the $Bi_{90}Sb_{10}$ layer sputtered from a single target. Furthermore, we increased the thickness of CoFeB to 1 nm to disintegrate the coupling between the MgO and Ta layer [23] but still

preserve the PMA from Ta/CoFeB/MgO trilayers. From the parallel conduction model, we expect that 38% of the applied current density flows into the BiSb layer in sample B. The post annealing treatment for the sample B is identical to the process applied to series of samples A. Then, we fabricated 20 μm cross Hall bars onto the film using optical lithography and ion milling process. Finally, we deposited thick contact electrodes of 15 nm Ta/5 nm Pt for the Hall bar. Figure 5.6 (b) shows an optical image of a cross Hall bar device and the configuration for SOT magnetization switching.

First of all, we reconfirmed the PMA characteristics of sample B in Figure 5.6 (c) and (d) by measuring R_{AHE} of the Hall bar device under H_{z} and H_{x}, respectively. We obtained $H_{\mathrm{k}} = 1.7\,\mathrm{kOe}$ for sample B by fitting the data in Figure 5.6 (d) using Equation (5.2). This H_{k} is slightly higher than that of sample A-2 with the same t_{CrO_x}. Next, Figure 5.6 (e) shows $R_{\mathrm{H}}^{2\omega}$ of sample B as a function of H_{x} measured at various current densities $J_{\mathrm{BiSb}} = 0.38,\ 0.45,\ 0.52,\ 0.58\,\mathrm{MA/cm^2}$. Finally, Figure 5.6 (f) shows the extracted H_{AD} as a function of J_{BiSb}, from which we obtained $\theta_{\mathrm{SH}} = 2.8$ for sample B. Further discussion on the difference of BiSb electrical conductivity and spin Hall angle between sample A-2 and sample B is provided at the end of this chapter.

Next, we performed the SOT magnetization switching induced by 50 μs pulse currents under various bias H_{x}, from $-275\,\mathrm{Oe}$ to $275\,\mathrm{Oe}$ as shown in Figure 5.7. The reversal of the switching loops when the H_{x} direction flips confirms that the magnetization switching was governed by SOT mechanism. Furthermore, the peak-to-peak amplitude of the R_{AHE} in the switching loops is consistent with that in Figure 5.6 (c), indicating full SOT magnetization switching in this sample. Moving forwards, we conducted the SOT magnetization switching triggered by pulse currents with various pulse widths τ_{pulse} from 50 μs to 10 ms under a fixed bias $H_{\mathrm{x}} = -275\,\mathrm{Oe}$ as shown in Figure 5.8. For further comparison, here we define the threshold switching current density, $J_{\mathrm{th}}^{\mathrm{BiSb}}$ as the current density in BiSb at which R_{AHE} crosses zero Ω. In the case of $\tau_{\mathrm{pulse}} = 50$ μs, $J_{\mathrm{th}}^{\mathrm{BiSb}}$ is approximately $3.1\,\mathrm{MA/cm^2}$. To demonstrate the superiority of BiSb over other HMs in ultra-low power operation, we also sputtered a reference sample with the structure of Ta (3.0 nm)/$Co_{20}Fe_{60}B_{20}$ (1.0 nm)/MgO (2.0 nm)/Ta (2.0 nm) under identical condition and performed the SOT magnetization switching. We

found that Ta requires a threshold of as much as $J_{\mathrm{th}}^{\mathrm{Ta}} = 20\,\mathrm{MA/cm^2}$ for $\tau_{\mathrm{pulse}} = 50$ μs just to switch 60% of the magnetization. Hence, we confirmed that BiSb can enable a lower switching current density by an order of magnitude compared with that in HM.

We now examined the thermal stability Δ of the sample B. In Figure 5.9 (a), we shows $J_{\mathrm{th}}^{\mathrm{BiSb}}$ as a function of reduced $\tau_{\mathrm{pulse}}/\tau_0$ with $\tau_0^{-1} = 1\,\mathrm{GHz}$ ($\tau_0 = 1\,\mathrm{ns}$) is the attempt switching frequency. The dashed lines shown in Figure 5.9 (a) are theoretical fittings using the following thermal activation model [24]

$$J_{\mathrm{th}}^{\mathrm{BiSb}} = J_0^{\mathrm{BiSb}} \times \left[1 - \frac{1}{\Delta} \log\left(\frac{\tau_{\mathrm{pulse}}}{\tau_0}\right)\right]. \tag{5.6}$$

The fittings give $J_0^{\mathrm{BiSb}} = 5.1\,\mathrm{MA/cm^2}$ and $\Delta = 27$. The physical meaning of Δ represents the energy barrier of the volume with size equal to the domain wall width. In other words, Δ is the energy barrier to nucleate a domain wall, rather than the energy barrier for coherently switching the whole volume of the magnetic layer [25]. However, Δ of sample B is about two-thirds of a typical $\Delta = 38$ for CoFeB/MgO [25] due to the smaller H_{k} of sample B. Next, we verified the SOT robustness of the sample B through the repeated SOT magnetization switching using a pulse sequence shown in Figure 5.9 (b) where pulse currents with amplitude of $2.6\,\mathrm{MA/cm^2}$ at 100 μs were applied to switch the magnetization followed by a small DC current for R_{AHE} readout. Figure 5.9 (c) shows R_{AHE} measured after each writing pulse under a bias H_{x} of $-275\,\mathrm{Oe}$ after 150 pulse counts. We successfully demonstrated the robustness of SOT switching by showing the unchanged device characteristics throughout the repeated switching which implies that the BiSb/CrO_x/Ta/CoFeB/MgO/Ta junction fabricated by the magnetron sputter is a potential candidate for SOT-MRAM cache memory.

5.3.3 Benchmarking of SOT power consumption

To provide more insight on the SOT power consumption of sample B compared to that of other SOT materials, including HMs, i.e., W, Pt, and Ta, and TIs, i.e., MBE-grown $(BiSb)_2Te_3$, we simply adopted the bilayer model [29] in which shunting current is taken into account for benchmarking. In a practical SOT-MRAM, the MTJ stack is milled into a pillar

SOT Material	**W** [26]	**Pt** [27]	**Ta** [2]	**$(BiSb)_2Te_3$ (MBE)** [28]	**BiSb (sputtered)**
Interfacial layers	-	-	-	Ti (2 nm)	CrO_x (1 nm)/ Ta (0.8 nm)
$\lvert\theta_{SH}\rvert$	0.21	0.12	0.15	2.5	2.8
σ_{SOT} ($10^5\ \Omega^{-1}\ m^{-1}$)	2.7	21	5.6	0.18	1.3
t_{SOT} (nm)	5	5	8	6	10

Table 5.1: Benchmarking of SOT for different materials.

on the SOT track as schematically shown in Figure 5.10 (a). In this model, the SOT power consumption P_{SOT} is given by the relationship

$$P_{SOT} \propto \frac{\sigma_{FM} t_{FM} + \sigma_{int} t_{int} + \sigma_{SOT} t_{SOT}}{(\sigma_{SOT} t_{SOT} \theta_{SH})^2}. \tag{5.7}$$

Here we assume a 1 nm thick CoFeB with $\sigma_{FM} = 6 \times 10^5\,\Omega^{-1}m^{-1}$ is deposited as the FM layer, and the interfacial layers are required when the SOT track is TIs. The parameters, including the magnitude of θ_{SH}, conductivity σ_{SOT}, and thickness t_{SOT} of the SOT materials, are shown in Table 5.1. In our sample, we use $\sigma_{Ta} = 4.06 \times 10^5\,\Omega^{-1}m^{-1}$ [30]. Figure 5.10 (b) shows the log-scale normalized power consumption P_{SOT}/P_W of different SOT materials. One can see that the power consumption from BiSb is about three orders of magnitude smaller than that of other HMs thanks to a large θ_{SH}. It is also worth noticing that even though $(BiSb)_2Te_3$ has a large θ_{SH} of 2.5, its power consumption is still approximately 500 times higher than that of BiSb. This is due to the fact that $(BiSb)_2Te_3$ exhibits a low conductivity and a large portion of writing current is shunted into the Ti interfacial layer and CoFeB. In such a case, higher writing current can increase Joule heating, which leads to the reduction of device lifetime as well as a low reliability for the SOT track [31]. Hence, for ultralow-power SOT-MRAM

applications, inserting a 1 nm CrO_x interfacial layer with high spin transparency can prevent shunting current and guarantee a large θ_{SH} and a good σ_{BiSb}.

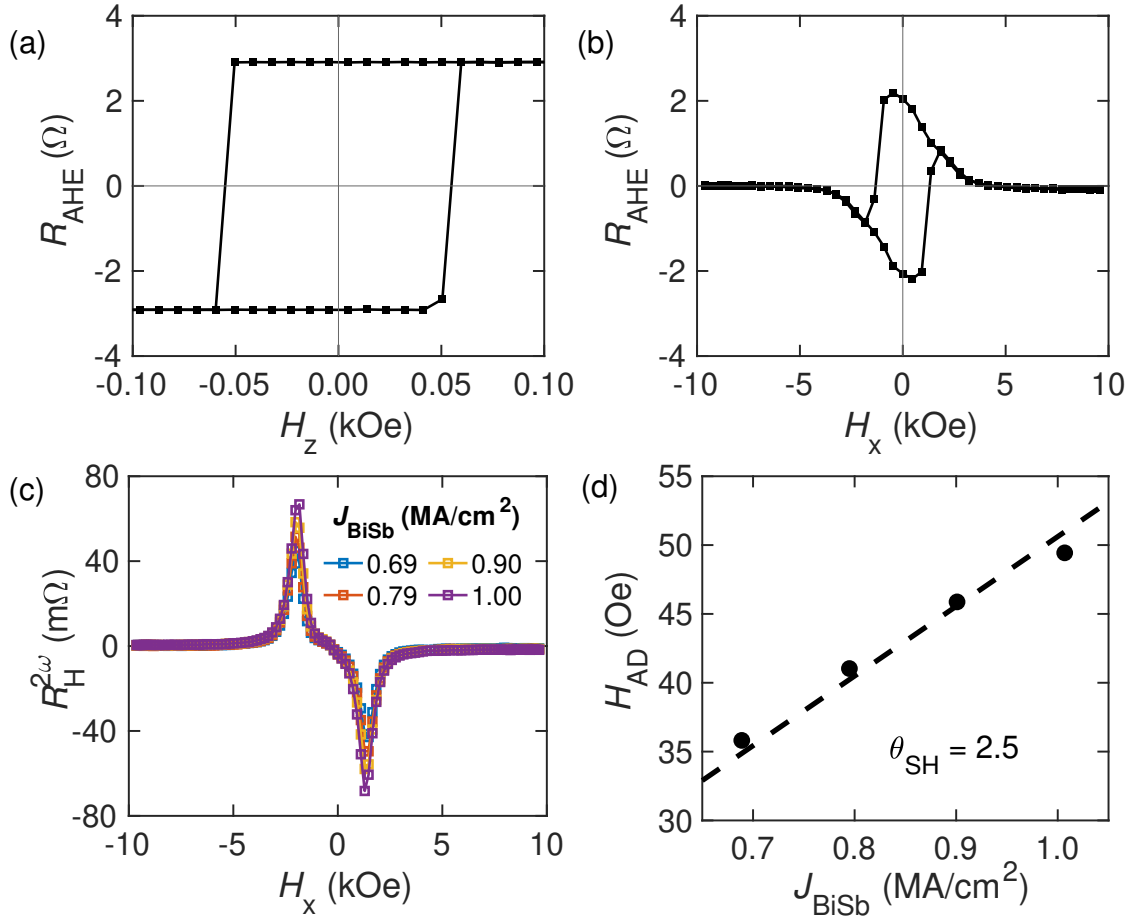

Figure 5.3: Representative sample A-2 with a 1.0 nm thick CrO_x layer. (a), (b) Anomalous Hall resistance of a Hall bar measured with an out-of-plane magnetic field H_z and an in-plane magnetic field H_x, respectively. (c) Second harmonic Hall resistance as a function of the in-plane external magnetic field H_x at different BiSb current densities. (d) Antidamping-like field H_{AD} as a function of J_{BiSb}.

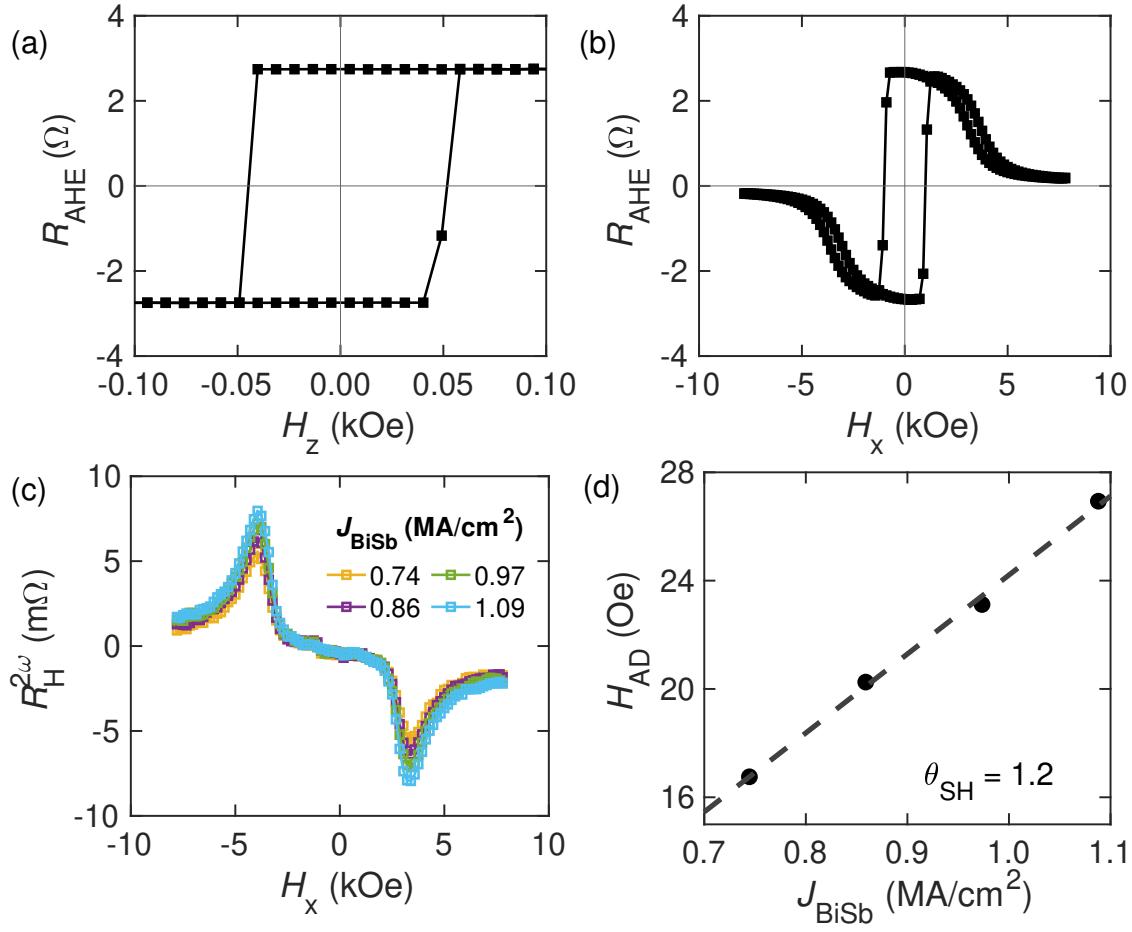

Figure 5.4: Representative sample A-5 with a 2.5 nm thick CrO_x layer. (a), (b) Anomalous Hall resistance of a Hall bar measured with an out-of-plane magnetic field H_z and an in-plane magnetic field H_x, respectively. (c) Second harmonic Hall resistance as a function of the in-plane external magnetic field H_x at different BiSb current densities. (d) Antidamping-like field H_{AD} as a function of J_{BiSb}.

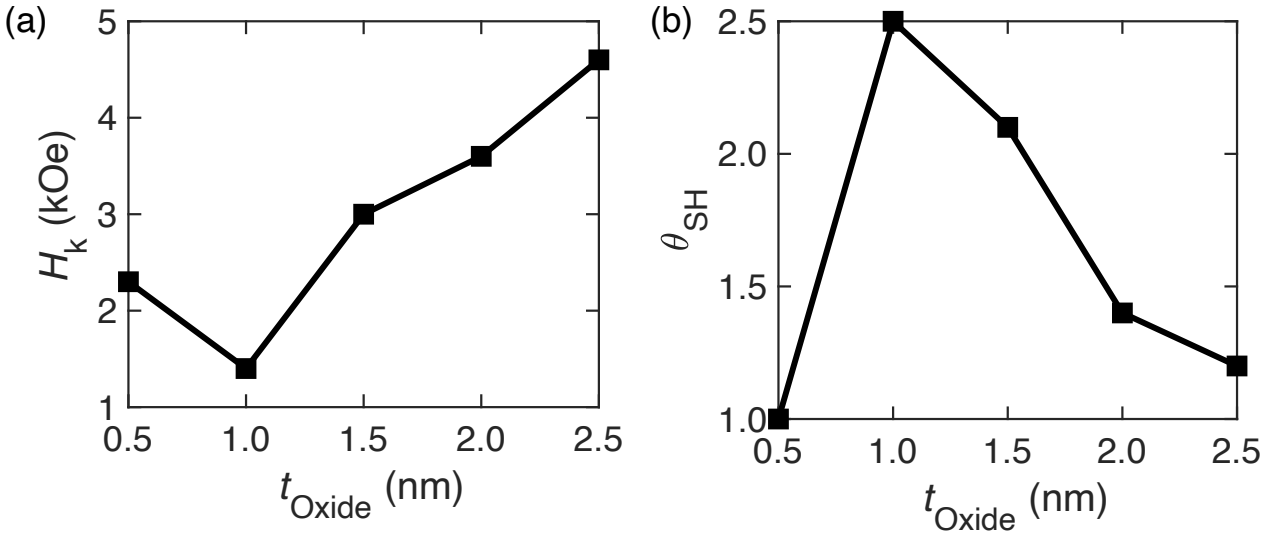

Figure 5.5: (a) H_{k} and (b) θ_{SH} as functions of the CrO_x interfacial layer thickness.

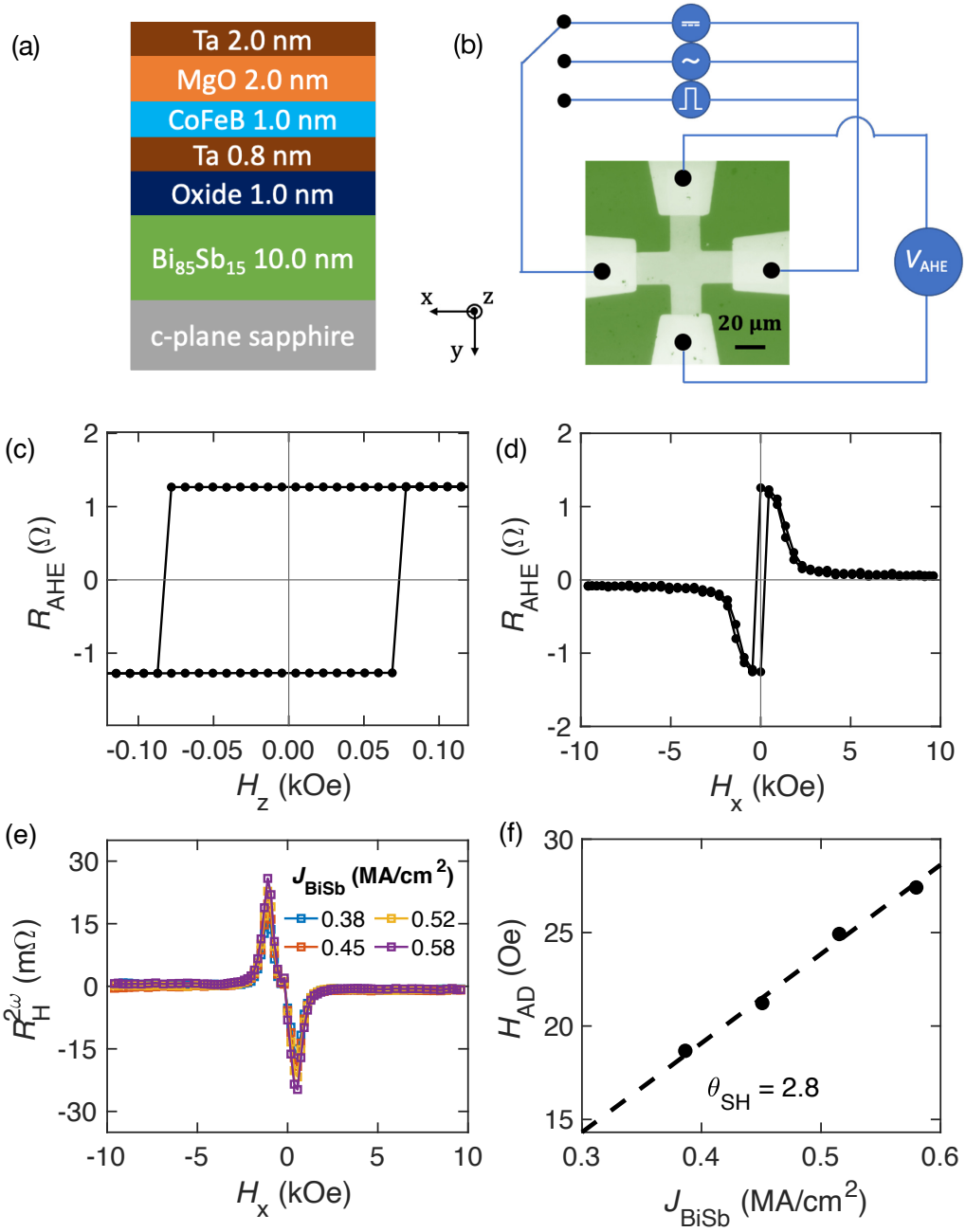

Figure 5.6: (a) Schematic stacking structure. (b) Optical image of a cross Hall bar device and measurement setup. (c), (d) Anomalous Hall resistance of a Hall bar measured with an out-of-plane magnetic field H_z and an in-plane magnetic field H_x, respectively. (e) Second harmonic Hall resistance as a function of the in-plane external magnetic field H_x at various BiSb current densities. (f) Antidamping-like field H_{AD} as a function of J_{BiSb}.

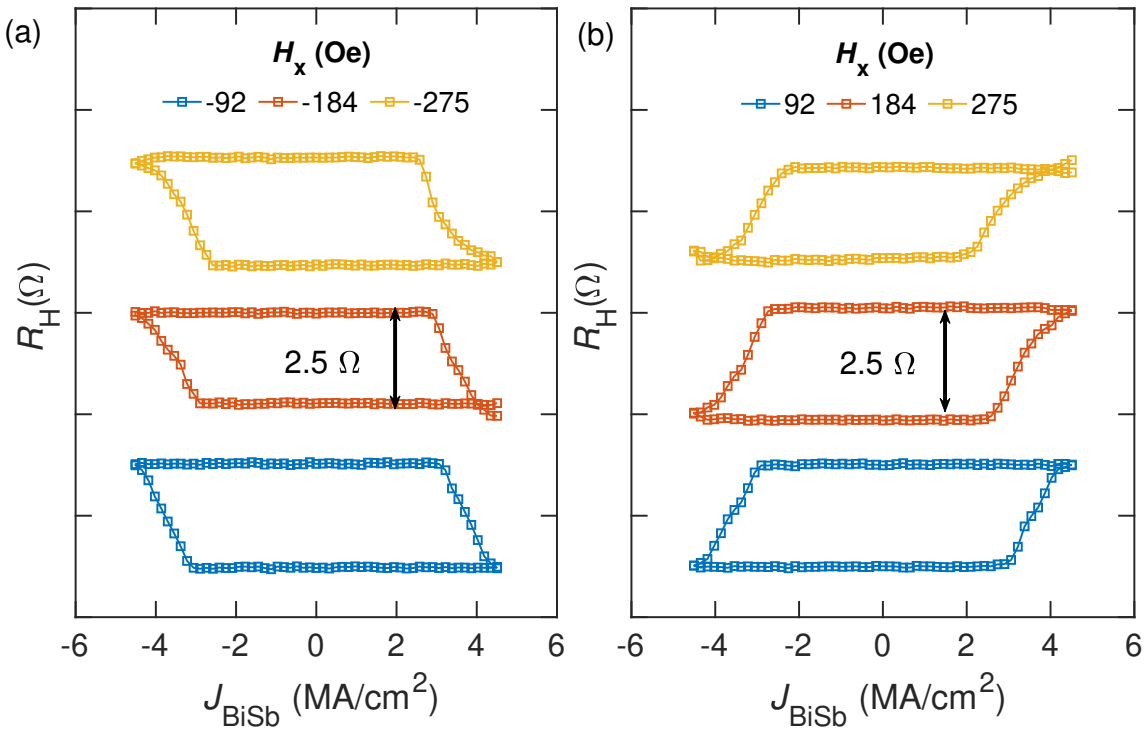

Figure 5.7: SOT switching loops induced by 50 μs pulse currents under various in-plane bias magnetic fields applied along (a) $-x$ direction and (b) $+x$ direction.

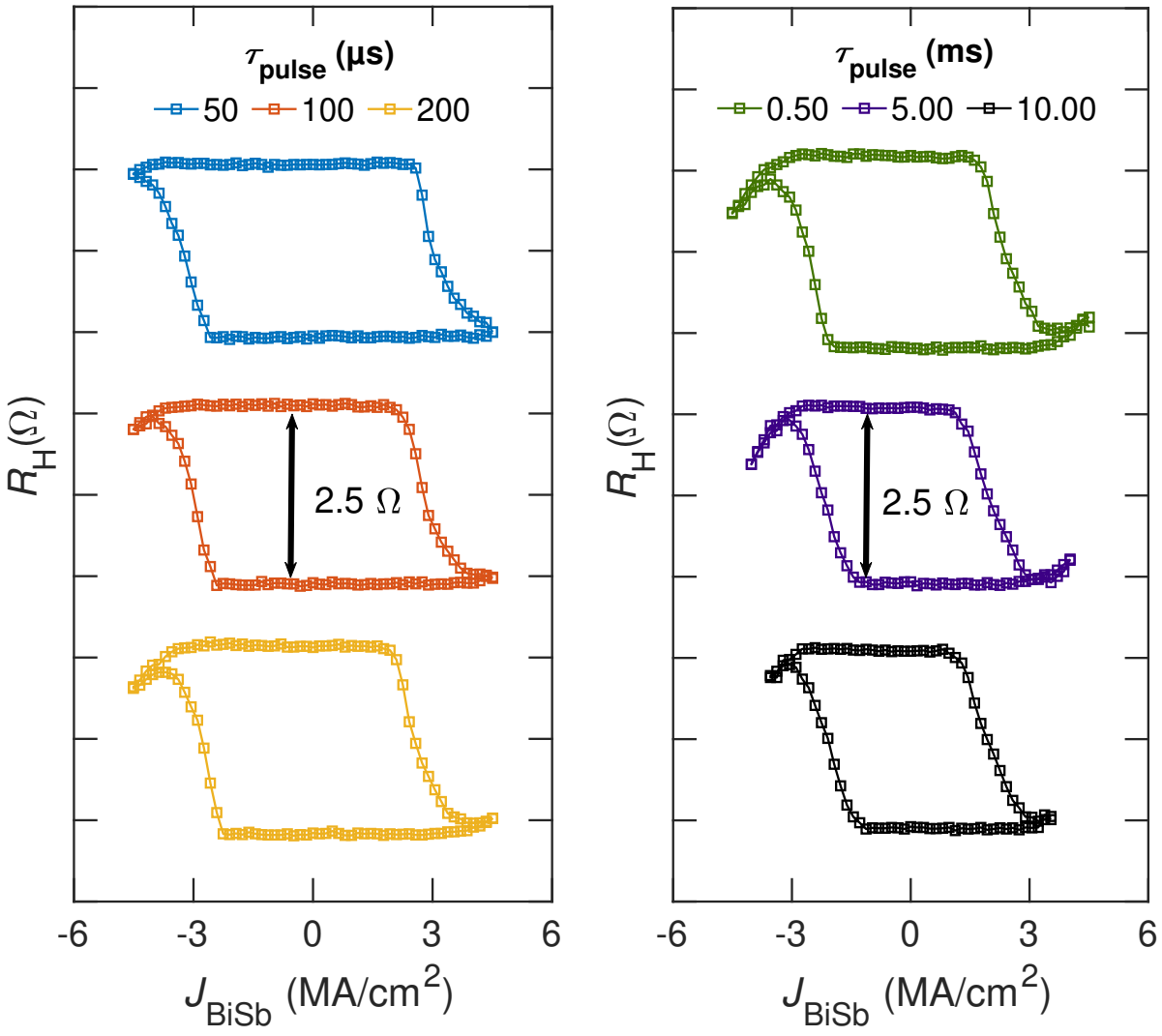

Figure 5.8: SOT magnetization switching loops by 50 μs, 100 μs, and 200 μs (left panel), and 0.5 ms, 5.0 ms, and 10.0 ms (right panel) pulse currents measured under a fixed $H_x = -275$ Oe.

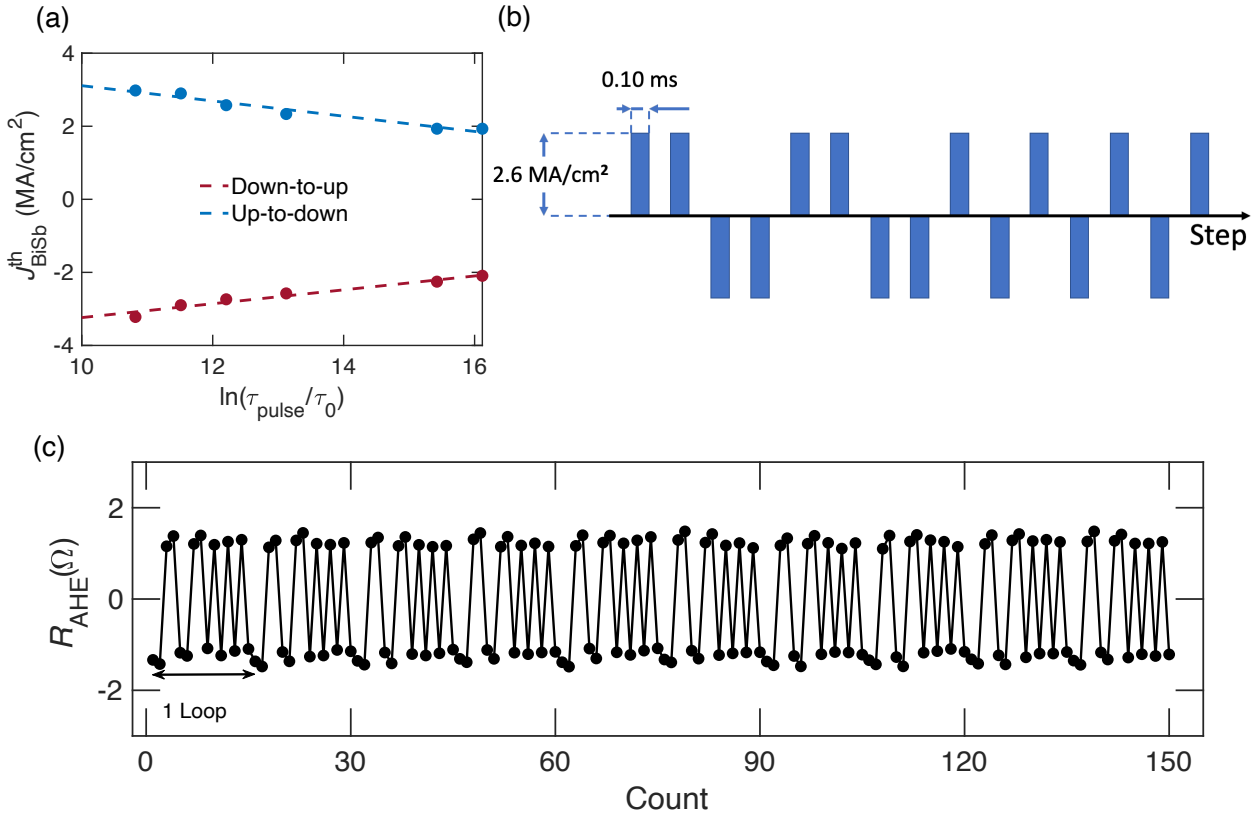

Figure 5.9: (a) BiSb threshold switching current density as a function of τ_{pulse}. (b) Pulse sequence for repeated SOT magnetization switching. (c) R_{AHE} measured by a small DC current after each writing pulse under a bias magnetic field of -275 Oe.

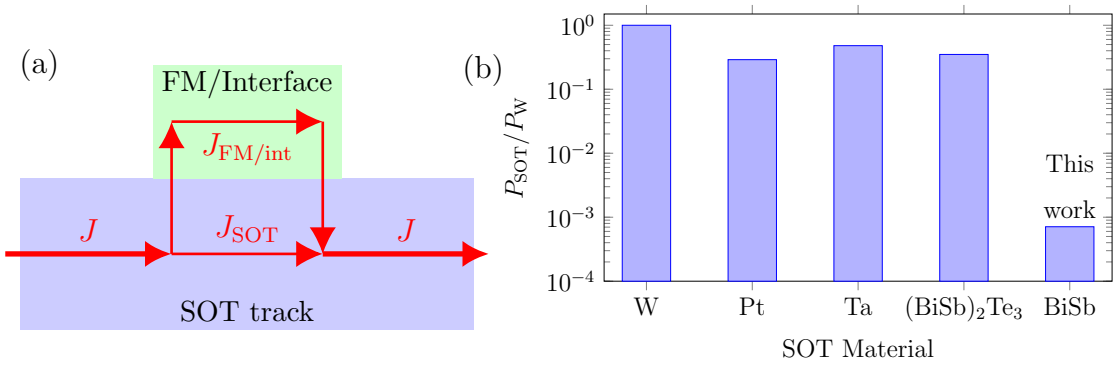

Figure 5.10: (a) A schematic of bilayer model for SOT-MRAM power consumption benchmarking. (b) The normalized SOT power consumption of several SOT materials.

5.4 Discussion

5.4.1 Bit retention time

To confirm that our device can hold a bit long enough for cache memory applications, we first examine the mechanism of data eviction in volatile caches to estimate how frequently cache need to discard data. In conventional computing, the average memory access time (AMAT) quantifies the average time the CPU takes to access data, considering the hierarchical nature of caches. The AMAT can be expressed as:

$$\text{AMAT} = T_{\text{L1}} + MR_{\text{L1}} \times \left[T_{\text{L2}} + MR_{\text{L2}} \times \left(T_{\text{L3}} + MR_{\text{L3}} \times T_{\text{mem}}\right)\right], \tag{5.8}$$

where:

- $T_{\text{L1}}, T_{\text{L2}}, T_{\text{L3}}$ are the access times for L1, L2, and L3 caches, respectively,
- T_{mem}: Main memory access time,
- $MR_{\text{L1}}, MR_{\text{L2}}, MR_{\text{L3}}$ are the miss rates for L1, L2, and L3 caches.

Here, we assume:

$$\begin{aligned} MR_{\text{L1}} = 5\%,\ MR_{\text{L2}} = 20\%,\ MR_{\text{L3}} = 10\%, \\ T_{\text{L1}} = 1\,\text{ns},\ T_{\text{L2}} = 10\,\text{ns},\ T_{\text{L3}} = 30\,\text{ns}, \\ T_{\text{mem}} = 100\,\text{ns}. \end{aligned}$$

Substituting these values into Equation (5.8), we can obtain an AMAT of 1.9 ns.

Afterwards, new data will be fetched into L1 cache. The access processes are repeated until the cache is full and start the eviction process. For an L1 cache of 128 KB with a block size of 64 bytes and an access speed of 1 GHz, this filling time can be estimated by:

$$\tau_{\text{fill}} \approx \frac{\text{Cache Size}}{\text{Block Size} \times \text{Access Speed}} = \frac{128 \times 1024}{64 \times 10^9} = 2.048\ \mu\text{s}. \tag{5.9}$$

Finally, the retention time before data eviction $\tau_{\text{retention}}$ can be calculated by adding AMAT, τ_{fill} and a data transmission time between buses τ_{bus}. As the bus speed is very fast,

up to few tens of GB/s, compared to the access speed of 1 GHz, we ignore the τ_{bus} and obtain $\tau_{\text{retention}}$ for $N = 10^6$ accesses via:

$$\tau_{\text{retention}} \approx \text{AMAT} \times N + \tau_{\text{fill}} \approx 1.9\,\text{ns} \times 10^6 + 2.048\ \mu\text{s} \approx 1.902\,\text{ms}. \tag{5.10}$$

Using the hierarchical nature of caches and realistic miss penalties at each level to estimate memory latency, we obtain a $\tau_{\text{retention}} \approx 1.902\,\text{ms}$.

In the case of non-volatile MRAM, the bit retention can be calculated via the thermal stability via:

$$\tau_{\text{retention}} = \tau_0 \exp\{\Delta\}. \tag{5.11}$$

With an assumption of $\tau_0 = 1$ ns, the $\Delta = 27$ yields a retention time of 500 seconds in nano-scale SOT-MRAM. With the above estimation with volatile cache, our retention time may allow up to 2.63×10^5 times of data eviction, which may be sufficient for CPU L1-cache memory applications.

As for lower cache memory such L3, a $\Delta = 38$ can retain the data for approximately 1 years. Further engineering solution should be considered to increase the thermal stability. One solution is employing a ferromagnetically coupled dual interface CoFeB/MgO as free layer which can significantly enhance the thermal stability without increasing the threshold switching current density [32].

5.4.2 Difference between $Bi_{90}Sb_{10}$ and $Bi_{85}Sb_{15}$ conductivity

In this part, we address the difference between $Bi_{85}Sb_{15}$ and $Bi_{90}Sb_{10}$ conductivity and possible influence on the threshold switching current density between sample B and A-2. From the control samples, the conductivity of $Bi_{90}Sb_{10}$ ($1.8 \times 10^5\,\Omega^{-1}\text{m}^{-1}$) is higher than that of $Bi_{85}Sb_{15}$ ($1.3 \times 10^5\,\Omega^{-1}\text{m}^{-1}$), and thus allows more current flowing into $Bi_{90}Sb_{10}$ than into $Bi_{85}Sb_{15}$. This enhancement can be explained by decomposing the conductivity of BiSb into the surface and bulk states conductivity:

$$\sigma_{\text{BiSb}} = \frac{\sigma^{\text{BiSb}}_{\text{surface}}}{t^{\text{BiSb}}_{\text{surface}}} + \sigma^{\text{BiSb}}_{\text{bulk}} = \frac{\sigma^{\text{BiSb}}_{\text{surface}}}{t^{\text{BiSb}}_{\text{surface}}} + \sigma_0 \exp\left(-\frac{E_g}{2k_B T}\right). \tag{5.12}$$

Since $Bi_{90}Sb_{10}$ possesses smaller bulk band gap comparing to that of $Bi_{85}Sb_{15}$, which can increase bulk intrinsic carriers [22], from this equation, higher conductivity is expected in $Bi_{90}Sb_{10}$ than in $Bi_{85}Sb_{15}$. However, in the case of 10 nm thin BiSb film, the TSSs dominantly contribute to the giant θ_{SH} whereas the bulk states in BiSb do not make an impact on generating pure spin current [13]. As a result, even though there is larger amount of currents flowing into $Bi_{90}Sb_{10}$ than into $Bi_{85}Sb_{15}$, they simply leak into the bulk and do not contribute to the generation of spin-orbit torque. This is supported by fact that there is higher $\theta_{SH} = 2.8$ for $Bi_{85}Sb_{15}$ compared with $\theta_{SH} = 2.5$ for $Bi_{90}Sb_{10}$ in samples with a 1.0 nm thick CrO_x. Hence, we expect no significant change in the threshold switching current density between $Bi_{90}Sb_{10}$ and $Bi_{85}Sb_{15}$.

5.5 Conclusion

In conclusion, we have studied the PMA and SOT characteristics in $Bi_{90}Sb_{10}$ (10.0 nm)/CrO_x (0.5 $\sim$ 2.5 nm)/Ta (0.8 nm)/$Co_{20}Fe_{60}B_{20}$ (0.9 nm)/MgO (2.0 nm)/Ta (2.0 nm) deposited by magnetron sputtering on c-plane sapphire substrate. We found that inserting a 1.0 nm CrO_x layer in between BiSb and the trilayers Ta/CoFeB/MgO could maintain PMA after thermal annealing and yield a relatively large effective $\theta_{SH} = 2.5$. Furthermore, we achieved a larger θ_{SH} of 2.8 in the sputtered $Bi_{85}Sb_{15}$ (10.0 nm)/CrO_x (1.0 nm)/Ta (0.8 nm)/$Co_{20}Fe_{60}B_{20}$ (1.0 nm)/MgO (2.0 nm)/Ta (2.0 nm) with PMA, and demonstrated the full SOT magnetization switching with a switching current density of 3.1 MA/cm^2, which is smaller than that in HMs by an order of magnitude. Our work shows that BiSb can be integrated into CoFeB/MgO with PMA for SOT-MRAM cache memory by inserting an oxide interfacial layer.

However, to reach out the manufacturability of BiSb, it is essential to achieve highly textured or epitaxial BiSb on amorphous substrate using current BEOL CMOS process. This process typically includes high temperature work at 400°C which is higher than the melting point of BiSb ($\approx$ 280°C). In the next chapter, we provided solutions for this issue.

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Chapter 6: Large spin-orbit torque induced by high temperature annealed BiSb topological insulator on oxidized Si substrate substrates

From previous chapters, BiSb has demonstrated significant potential in various magnetic storage devices due to its strong SHE and ISHE. However, the manufacturability of BiSb remains questionable for SOT-MRAM application. The utmost concern is whether or not BiSb can be integrated into the current state-of-the-art CMOS, where process temperature far exceeds BiSb melting point. With such a harsh condition, the crystallinity of BiSb during mass manufacturing on silicon wafers remains uncertain. This is a crucial issue, as achieving high-performance BiSb with large θ_{SH} hinges on maintaining good crystallinity. In this chapter, we investigate the SHE of 400°C annealed BiSb in high-temperature-capable stacks that could be integrated with the CMOS process. By employing oxide buffer and seed layers in addition to a protection layer for BiSb, we could melt and recrystallize BiSb into a single phase with a large spin Hall angle of up to 7.6. We can also perform the SOT magnetization switching with a small current of 1.3 MA/cm^2 at 50 μs even after the high-temperature process is completed. Our finding indicates the potential of integrating BiSb with CMOS electronics for the mass production of BiSb-based SOT-MRAM and other magnetic memory applications.

6.1 Introduction

The recent progress on SOT-MRAM has proven its potential as the next-generation non-volatile memory technology with remarkable high-speed operation, excellent endurance, and low power consumption. As semiconductor scaling reaches its physical limits, SOT-MRAM has emerged as a promising alternative to traditional memory technologies, addressing both performance and energy efficiency challenges.

One of the critical advancements enabling the integration of SOT-MRAM into modern electronic devices is its compatibility with the BEOL fabrication processes used in CMOS technology. BEOL processes, typically involving the deposition and patterning of interconnects and thin-film materials at a large temperature budget, can achieve seamless CMOS electronic integration. This compatibility guarantees the low-cost manufacturing of SOT-MRAM alongside existing technologies, without disrupting established fabrication workflows. Among the significant development in SOT-MRAM fabrication is the use of W-based materials as a spin current injector [1]. W's unique properties, such as a larger spin Hall angle of 0.4 compared to Ta or Pt and its high temperature budget, have made it a preferred choice for SOT-MRAM devices [2]. Recently, a 300 mm Si wafer of W-based SOT-MRAM showed a switching current of 680 μA at 2 ns, a TMR ratio of up to 119%, very high endurance of about 10^{12} cycles, and great uniformity with a yield of 99.6% [3].

However, the spin Hall conductivity, defined as the product of θ_{SH} and σ, of W (1.9×10^5 $\hbar/2e$ Ω^{-1} m^{-1}) remains limited in comparison to those of sputtered Bi-based TIs such as sputtered Bi_2Se_3 with 6.5×10^5 $\hbar/2e$ Ω^{-1} m^{-1} [4] and sputtered BiSb with the highest of 10.8×10^5 $\hbar/2e$ Ω^{-1} m^{-1} [5]. We expect spin Hall conductivities of at least nearly an order of magnitude for TIs compared with that in HMs, which can further reduce the power consumption of the SOT-MRAM. Unfortunately, the integration of Bi-based TIs into CMOS electronic processes remains uncertain due to their low melting point. At 300°C, Bi_2Se_3 already suffers from a severe decomposition as shown in Panel 7 of Figure 52 in Reference [6]. In reality, the BEOL process may require a high-temperature process up to 400°C, which is much higher than BiSb melting point of approximately 280°C. Such a harsh fabrication environment can

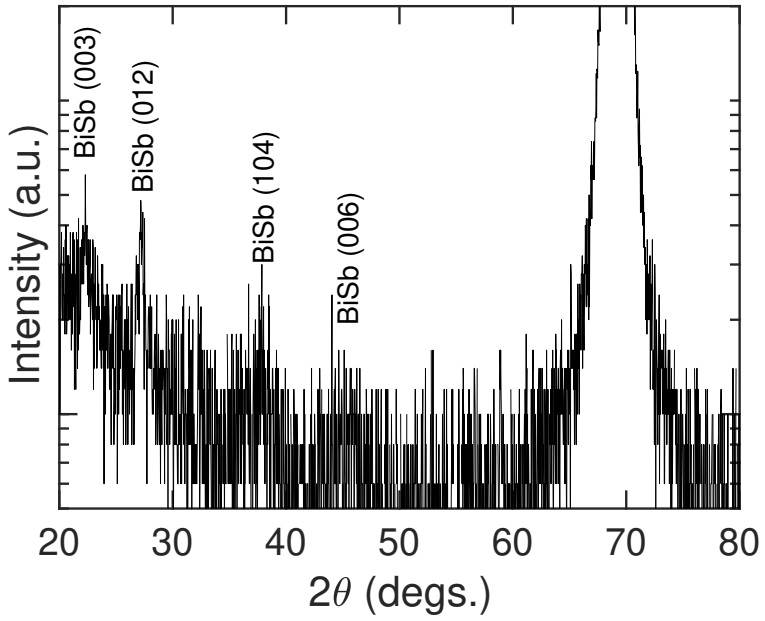

Figure 6.1: The out-of-plane XRD spectrum of sputtered BiSb (10 nm)/TiO_x (1.5 nm)/oxidized silicon substrate.

degrade the TSSs of BiSb, which is responsible for the strong SHE. Furthermore, to enhance the manufacturability, BiSb needs to be fabricated on amorphous Si/SiO_x. Nonetheless, the as-growth sputtered BiSb on oxidized silicon substrate often exhibits polycrystallinity. An example of out-of-plane XRD spectrum of room-temperature sputtered BiSb (10 nm)/TiO_x (1.5 nm)/oxidized silicon substrate, shown in Figure 6.1, displays a polycrystallinity with multiple phases. So far, achieving single-phase of BiSb with large spin Hall angle is only possible on crystallized substrates such as GaAs [7], c-plane sapphire [8], and BaF_2 [9].

In this work, we developed high-temperature-capable stacks using sputtered BiSb on oxidized silicon substrates. To induce the single phase, we melted and recrystallized BiSb using a 400° post annealing. To do so, here BiSb is sandwiched between oxide buffer/optional seed layers and a protection layer. The inserted buffer layer of TiO_x serves as the spacer from the thermally oxidized silicon layer and BiSb. This buffer can prevent oxygen diffusion, which could otherwise oxidize BiSb during the thermal work. Moreover, it can function as a control layer, facilitating the recrystallization of BiSb into a specific phase. The optional seed layer

of TaO_x may be required to support the recrystallization of BiSb. In general, oxide buffer and seed layers are preferred due to their high resistivity, which does not shunt the current. To protect BiSb from evaporation during high-temperature annealing at 400°C, we capped BiSb with a 3 nm Ti, which is known for its good spin transparency in junctions with BiSb [5]. After sandwiching BiSb between the buffer/seed and the protection layers, we anneal the stacks at 400°C to melt and recrystallize BiSb into a single phase. Here, we use either Pt/Co/Pt or Ta/CoFeB/MgO as the FM multilayers. By high-temperature annealing, we can improve the BiSb conductivity up to $1.2 \times 10^5\ \Omega^{-1}\ \mathrm{m}^{-1}$ and achieve a relatively large $\theta_{\mathrm{SH}} = 2.9 - 7.6$. Moreover, the SOT magnetization switching was also confirmed by using a BiSb current density as low as 1.3 $\mathrm{MA/cm^2}$ at 50 μs, which is an order of magnitude smaller than that in HMs. Our results show that utilizing oxide buffer/seed layers and post-annealing is an effective way to achieve high-performance BiSb on oxidized silicon substrates.

6.2 Melting and recrystallization of BiSb

6.2.1 Sample A

6.2.1.1 Sample preparation

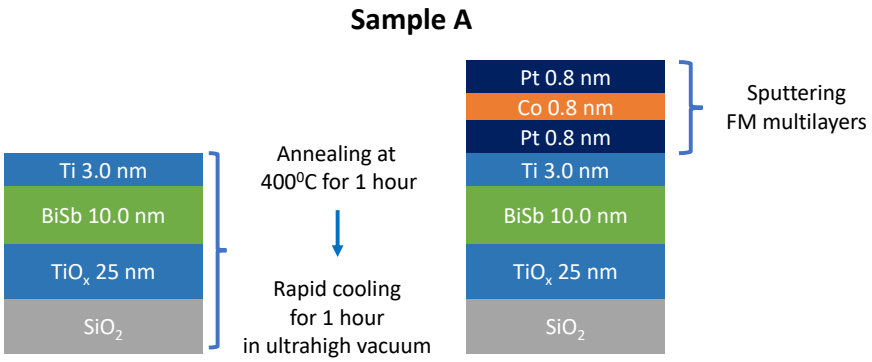

Figure 6.2: Detailed structure of sample A and the fabrication process.

Figure 6.2 shows the schematic structure of sample A and its fabrication process. At first, we sputtered 25 nm of buffer TiO_x from a single target Ti using Ar mixed with reactive O_2

gas. Afterwards, 10 nm of BiSb capped by 3 nm of Ti were deposited and annealed at 400°C for an hour in ultrahigh vacuum. After that, the sample was undergone a cooling process at room temperature in ultrahigh vacuum for one hour. Then, we sputtered the FM multilayers consisting of Pt (1 nm)/Co (1 nm)/Pt (1 nm) before taking the sample out of the sputtering system.

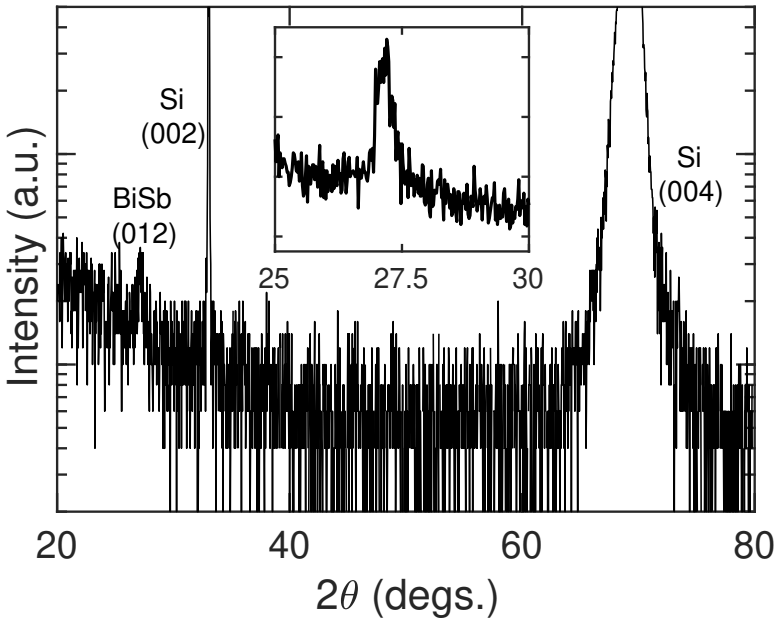

Figure 6.3: The wide-view (main figure) and narrow-view (inlet) out-of-plane XRD spectrum of sample A.

6.2.1.2 Sample characterization

To evaluate σ_{BiSb}, we adopted the same fabrication process as above to fabricate a control sample without Pt (1 nm)/Co (1 nm)/Pt (1 nm). By substracting the resistance of 3 nm Ti layer, the parallel resistor model yields a relatively high σ_{BiSb} of $1.2 \times 10^5\ \Omega^{-1}\ \mathrm{m}^{-1}$. Next, the 2θ wide-view and narrow-view out-of-plane XRD spectrum of sample A is shown in Figure 6.3, which reveals that BiSb was melted and recrystallized into single-phase BiSb (012). From the narrow-view of $2\theta = 25$–30 degree, the sharp peak of BiSb (012) ($2\theta = 27.20°$ and a full width at half maximum (FWHM) of $0.42°$) yields an out-of-plane grain size $G = 19.5$ nm by

using the Scherrer equation

$$G = \frac{K\lambda}{\beta \cos\theta}. \tag{6.1}$$

In this equation, K is the dimensionless shape factor with a typical value of 0.9 while β is the FWHM. For this XRD analyzer, the XRD source is CuKα with wavelength λ of 1.54 Å.

For the spin transportation measurement, we start with the R_{AHE} measurement to confirm the PMA of this sample. Figure 6.4 (a) and (b) show the R_{AHE} of the Hall bar device measured as a function of H_{z} and H_{x}, respectively. We failed to achieve a strong PMA in this case, which was confirmed by a round-corner hysteresis in Figure 6.4 (a) together with a weak PMA effective field in Figure 6.4 (b). Afterwards, Figure 6.4 (c) shows $R_{\mathrm{H}}^{2\omega}$ when scanning H_{x} using various current densities $J_{\mathrm{BiSb}} = 0.33,\ 0.40,\ 0.55,$ and 0.63 MA/cm^2. From this data, we extract the H_{AD} as a function of various J_{BiSb} by fitting the data with

$$R_{\mathrm{H}}^{2\omega} = \frac{R_{\mathrm{AHE}}}{2}\frac{H_{\mathrm{AD}}}{H_{\mathrm{x}} - H_{\mathrm{k}}} + R_{\mathrm{ONE}}H_{\mathrm{x}} + R_{\mathrm{ANE+SSE}}. \tag{6.2}$$

The extracted results are shown in Figure 6.4 (d), which gives a $\theta_{\mathrm{SH}} = 2.9$ obtained using the formula:

$$\theta_{\mathrm{SH}} = \frac{2e}{\hbar} t_{\mathrm{Pt/Co/Pt}} M_{\mathrm{s}} \frac{\partial H_{\mathrm{AD}}}{\partial J_{\mathrm{BiSb}}}, \tag{6.3}$$

where $t_{\mathrm{Pt/Co/Pt}} = 2.4$ nm and $M_{\mathrm{s}} = 613$ emu/cm^3 [10]. In conclusion, sample A was successfully melted and recrystallized into single-phase BiSb (012) with relatively high $\sigma_{\mathrm{BiSb}} = 1.2 \times 10^5\ \Omega^{-1}\ \mathrm{m}^{-1}$. However, a strong PMA could not be achieved in this sample. For ultrahigh bit density application, a p-MTJ is crucial. Thus, in the next part, we suggest the integration of CoFeB/MgO junction and a two-step annealing process to achieve the PMA on top of 400°C annealed BiSb.

6.2.2 Sample B

6.2.2.1 Sample preparation

Similar to sample A, at first, a thick 25 nm of TiO_x was sputtered from Ti target with Ar and O_2 gas. Here, an additional seed layer of TaO_x was inserted before sputtering 10 nm of BiSb and 3 nm of Ti protection layer. After that, the stack was annealed at 400°C

for an hour, and was left for cooling to room temperature in ultrahigh vacuum for one hour. Then, we sputtered the FM multilayers consisting of Ta (1nm)/$Co_{20}Fe_{60}B_{20}$ (1nm)/MgO (3 nm)/Ta (2 nm) and annealed the whole stack again at 250°C for 30 minutes to crystallize $Co_{20}Fe_{60}B_{20}$ into bcc-CoFe and to achieve PMA. Finally, sample B was cooled down for another one hour before transferring out of the sputtering system. The schematic structure and the corresponding fabrication process of sample B are illustrated in Figure 6.5.

6.2.2.2 Sample characterization

Here we found that after the first annealing process at 400°C for an hour, σ_{BiSb} was 1.0×10^5 Ω^{-1} m^{-1} which is slightly smaller than that of the sample A but is typical conductivity for sputtered BiSb on amorphous silicon substrate [11]. However, after the second annealing process to crystallize CoFeB at 250°C for 30 minutes, we could obtain only σ_{BiSb} of 0.5×10^5 Ω^{-1} m^{-1} , which is only half of the initial value. The halve of σ_{BiSb} may suggest a decrease of BiSb crystallinity. To confirm that, we show the out-of-plane XRD spectrum of sample B in Figure 6.6. From the narrow-view of 2θ = 20–30 degree, sample B was melted and recrystallized into single-phase BiSb (001) with a broad peak ($2\theta = 22.36$ and an FWHM of 2.21°). Using the Scherrer equation, we estimate the out-of-plane grain size of this sample is only 3.7 nm. This may contribute to the low σ_{BiSb} of sample B.

In the next characterization, we begin with the PMA evaluation of this device as shown in Figure 6.7 (a) and (b). Here, the R_{AHE} of the Hall bar device were measured while scanning H_{z} and H_{x}, respectively. By integrating 250°C annealed Ta (1 nm)/CoFeB (1 nm)/MgO (3 nm) instead of Pt (1nm)/Co (1nm)/Pt (1nm), we confirmed a clear PMA with $H_{\mathrm{k}} = 2.8\,\mathrm{kOe}$ obtained by fitting the data in Figure 6.7 (b) with:

$$R_{\mathrm{AHE}} = R_{\mathrm{AHE}}(0)\sqrt{1 - \left(\frac{H_{\mathrm{x}}}{H_{\mathrm{k}}}\right)^2}. \tag{6.4}$$

Then, Figure 6.7 (c) shows $R_{\mathrm{H}}^{2\omega}$ of this device as a function of H_{x} at different current densities $J_{\mathrm{BiSb}} = 0.20,\ 0.24,\ 0.28,$ and $0.32\ \mathrm{MA/cm^2}$ for the SOT characteristic evaluation. Here, we assume that the thickness of BiSb does not change during thermal annealing. Last, we extract the H_{AD} – J_{BiSb} relationship as shown in Figure 6.7 (d) by fitting the second harmonic curves

using Equation (6.2). From the slope of H_{AD} – J_{BiSb}, a large $\theta_{\mathrm{SH}} = 7.6$ is obtained using the formula:

$$\theta_{\mathrm{SH}} = \frac{2e}{\hbar} t_{\mathrm{CoFeB}} M_{\mathrm{s}} \frac{\partial H_{\mathrm{AD}}}{\partial J_{\mathrm{BiSb}}}, \tag{6.5}$$

with $t_{\mathrm{CoFeB}} = 1$ nm and $M_{\mathrm{s}} = 1800$ emu/cm^3.

6.2.2.3 Type-z SOT magnetization switching

To confirm the functionality of the device after the high temperature process, demostration on read and write capability is necessary. To do so, we performed the DC SOT magnetization switching at various bias H_{x}, from -0.37 kOe to 0.37 kOe as shown in the left panel of Figure 6.8. At $H_{\mathrm{x}} \approx 0$ kOe, there is no deterministic switching. As increasing the H_{x}, the type-z SOT magnetization switching was achieved at low $J_{\mathrm{th}}^{\mathrm{BiSb}} \approx 0.52$ MA/cm^2 and $H_{\mathrm{x}} = 0.18$ kOe. Here, the peak-to-peak amplitude of the switching loops is same as that of the R_{AHE} – H_{x} curve in Figure 6.7 (b), indicating the full SOT magnetization switching in sample B. Furthermore, SOT is the driving mechanism, indicated by the the reversal of the switching loops as the bias magnetic field flips back and forth between x and $-x$. The dependence of $J_{\mathrm{th}}^{\mathrm{BiSb}}$ on the bias H_{x} is summarized in the right panel of Figure 6.8. The relationship of $J_{\mathrm{th}}^{\mathrm{BiSb}}$ – H_{x} suggests that a higher input current is necessary to switch the magnetization when the bias field is weaker. Hence, this trend aligns with the macrospin model [12].

In the next experiment, we conducted the pulse SOT magnetization switching with different pulse widths τ_{pulse} from 50 µs to 10 ms under a fixed bias $H_{\mathrm{x}} = 0.46$ kOe as shown in Figure 6.9. With such a large θ_{SH} in this sample, we could achieve the SOT magnetization switching at $\tau_{\mathrm{pulse}} = 50$ µs using a $J_{\mathrm{th}}^{\mathrm{BiSb}}$ of approximately 1.3 MA/cm^2.

Finally, we examine the thermal stability of this device to verify the switching performance of CoFeB/MgO junction on top of 400°C annealed BiSb. In Figure 6.10, we shows $J_{\mathrm{th}}^{\mathrm{BiSb}}$ as a function of reduced $\tau_{\mathrm{pulse}}/\tau_0$ with $\tau_0^{-1} = 1$ GHz ($\tau_0 = 1$ ns) is the attempt switching frequency. The up and down panels display $J_{\mathrm{BiSb}}^{\mathrm{th}}$ of switching from $-m_z$ to m_z and back, respectively.

The dashed lines represents the theoretical fittings using the thermal activation model [13]

$$J_{\mathrm{th}}^{\mathrm{BiSb}} = J_0^{\mathrm{BiSb}} \times \left[1 - \frac{1}{\Delta} \log\left(\frac{\tau_{\mathrm{pulse}}}{\tau_0}\right)\right]. \tag{6.6}$$

The fittings give $J_0^{\mathrm{BiSb}} = 2.1\,\mathrm{MA/cm^2}$ and $\Delta = 35$. This $\Delta = 35$ agrees with the typical Δ for single CoFeB in junction with MgO [14], which indicates the robustness of our device after high-temperature exposure.

6.2.2.4 Spin Hall angle comparison

To see the improvement of θ_{SH} owing to the melting and recrystallization process, we compare θ_{SH} of sample B with that of previous works on crystallized sapphire substrate. Figure 6.11 shows θ_{SH} of $(\mathrm{BiSb})_2\mathrm{Te}_3$ grown by MBE on sapphire substrate [15], 250°C annealed BiSb with CrO_x interfacial layer in Chapter 5, 250°C annealed BiSb with metallic Ti interfacial layer [5], and 400°C annealed BiSb in this work. With a value of 7.6, sample B, fabricated by the sputtering method on oxidized silicon substrate, shows a three times larger θ_{SH} than that of MBE-grown $(\mathrm{BiSb})_2\mathrm{Te}_3$ and 250°C annealed sputtered BiSb in Chapter 5 on sapphire substrates. Furthermore, in Reference [5], the stack structure, consisting of sputtered BiSb/Ti (3 nm)/Ta (0.8 nm)/CoFeB (1 nm)/MgO (2.5 nm)/Ta (1 nm) on sapphire substrate, was annealed at 250°C and demonstrated $\theta_{\mathrm{SH}} = 6$. This stack structure, to some extent, is similar to sample B, except for the buffer TiO_x/seed TaO_x layers. Thanks to the use of a high-temperature-capable stack, θ_{SH} can even be increased by approximately 25%. This enhancement indicates that it is possible to fabricate BiSb using a high temperature process while preserving a large θ_{SH}.

In summary, we could achieve PMA in sample B by introducing FM multilayers Ta (1 nm)/CoFeB (1 nm)/MgO (3 nm)/Ta (1 nm) together with an additional 30 minutes 250°C annealing process. Melted and recrystallized BiSb (001) provided a large $\theta_{\mathrm{SH}} = 7.6$ and a low $J_{\mathrm{th}}^{\mathrm{BiSb}} = 1.3\ \mathrm{MA/cm^2}$ at 50 µs. However, the additional annealing may degrade BiSb crystallinity which results in a halve in σ_{BiSb} to $0.5 \times 10^5\ \Omega^{-1}\ \mathrm{m}^{-1}$.

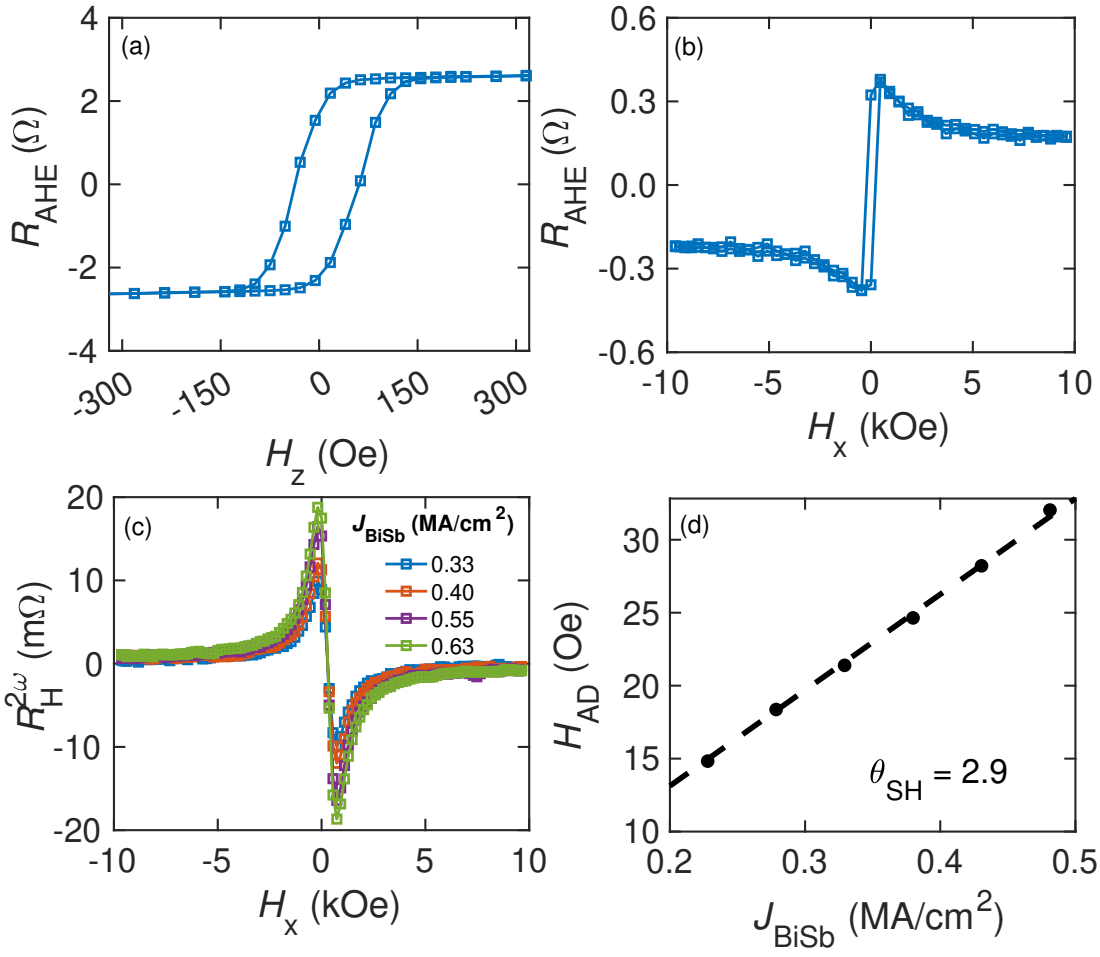

Figure 6.4: Characteristics of sample A. (a), (b) Anomalous Hall resistance of a Hall bar measured with an out-of-plane magnetic field H_z and an in-plane magnetic field H_x, respectively. (c) Second harmonic Hall resistance as a function of the in-plane external magnetic field H_x at different BiSb current densities. (d) Antidamping-like field H_{AD} as a function of J_{BiSb}.

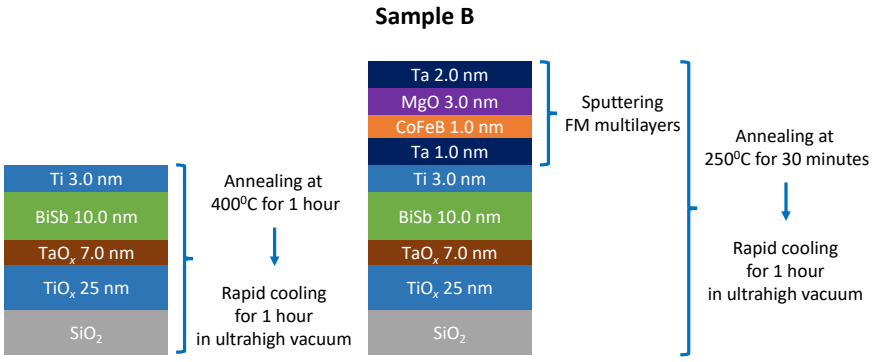

Figure 6.5: Detailed structure of sample B and the fabrication process.

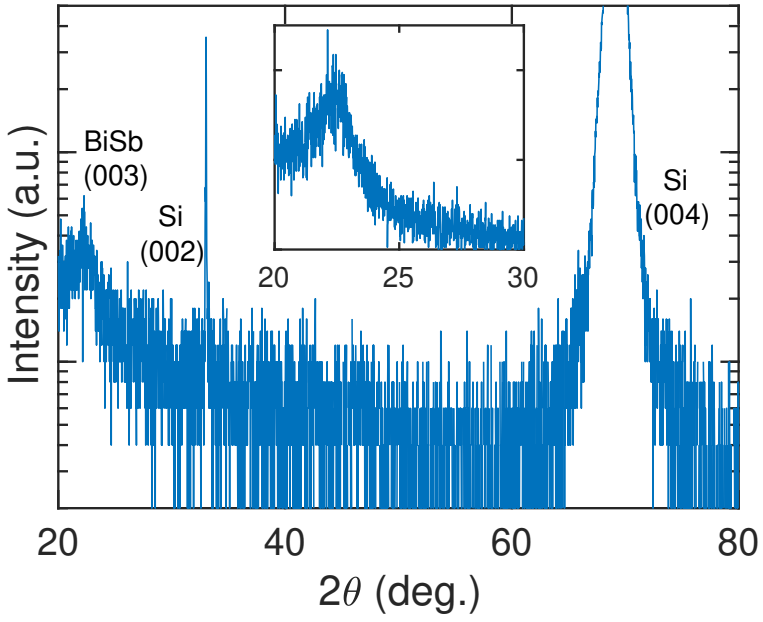

Figure 6.6: The wide-view (main figure) and narrow-view (inlet) out-of-plane XRD spectrum of sample B.

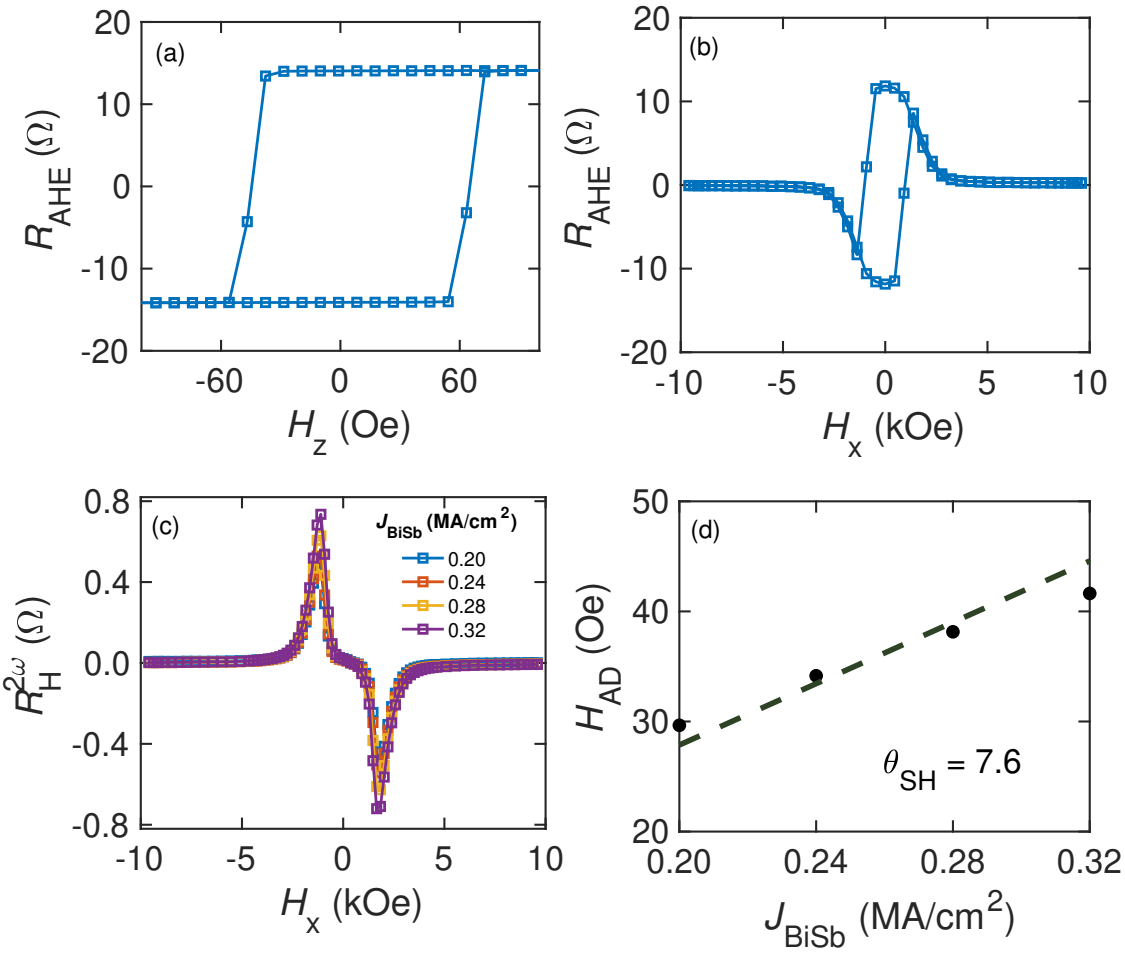

Figure 6.7: Characteristics of sample B. (a), (b) Anomalous Hall resistance of a Hall bar measured with an out-of-plane magnetic field H_z and an in-plane magnetic field H_x, respectively. (c) Second harmonic Hall resistance as a function of the in-plane external magnetic field H_x at different BiSb current densities. (d) Antidamping-like field H_{AD} as a function of J_{BiSb}.

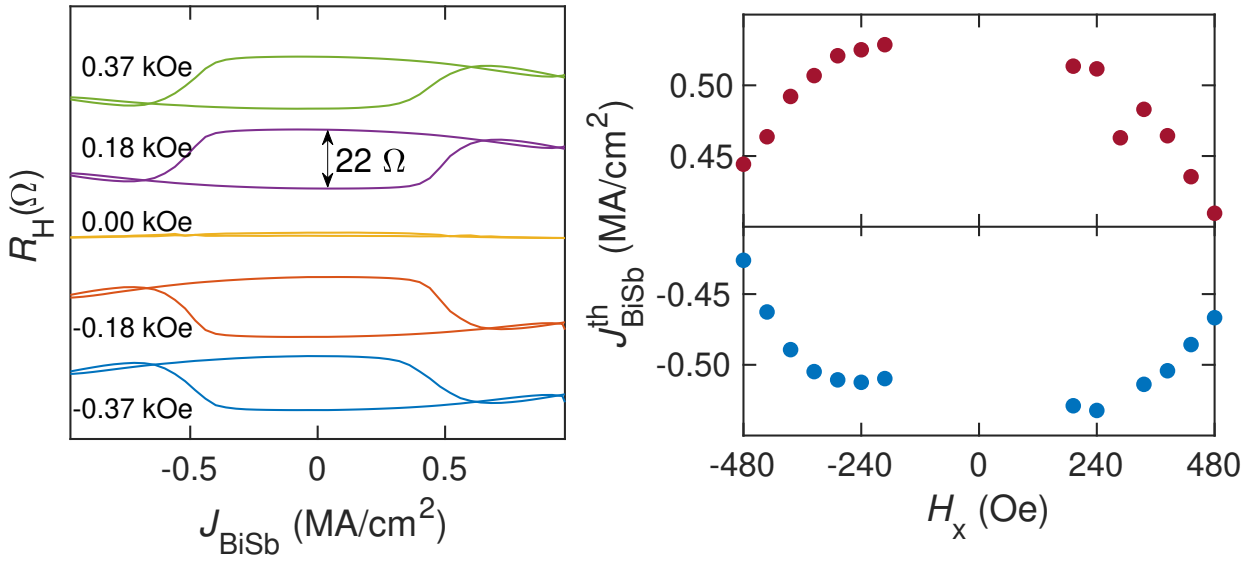

Figure 6.8: Representative SOT magnetization switching loops triggered by DC current under various H_x (left panel) and the dependence of BiSb threshold switching current densities on H_x (right panel).

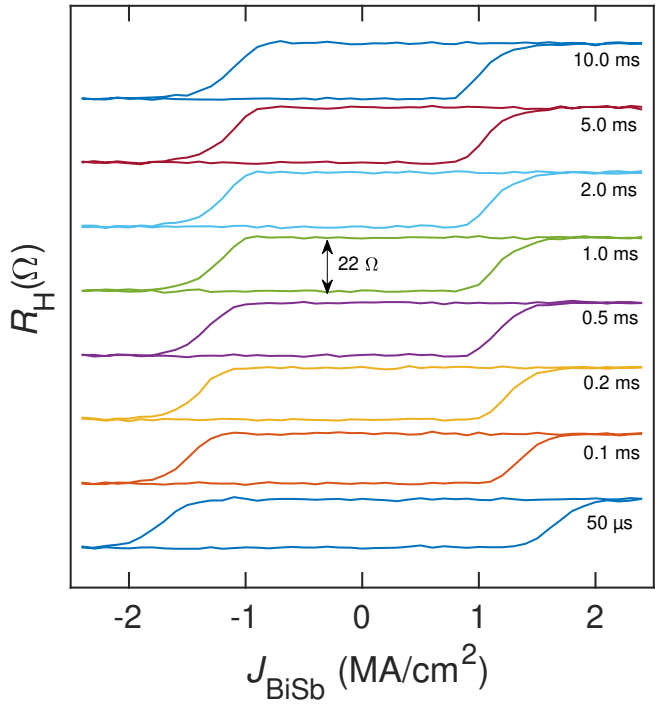

Figure 6.9: SOT magnetization switching loops by various pulse currents ranging from 50 μs to 10.0 ms under a fixed $H_x = -0.46$ kOe.

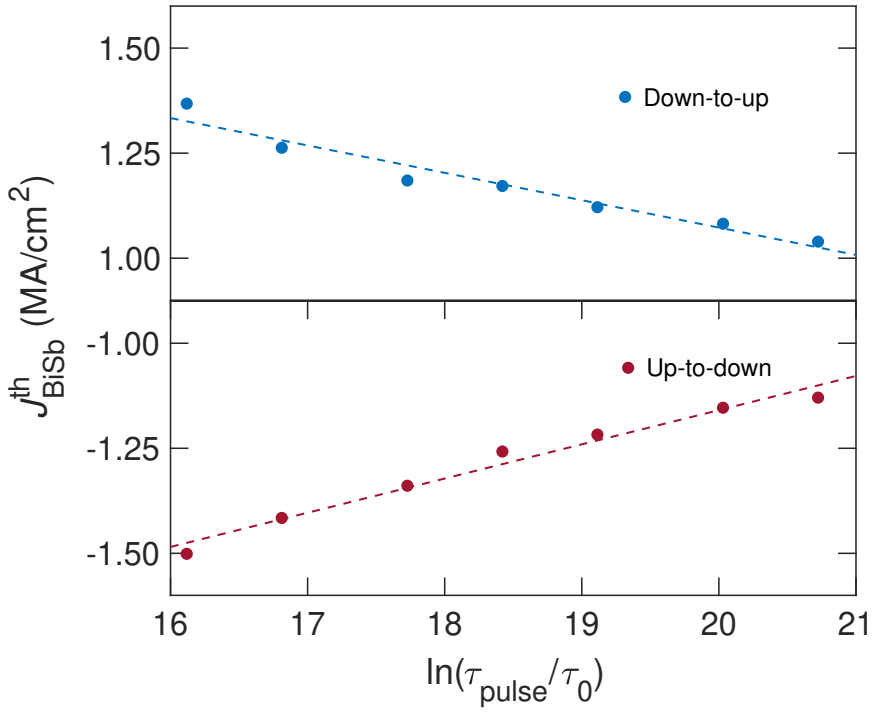

Figure 6.10: BiSb threshold switching current densities as a function of τ_{pulse}.

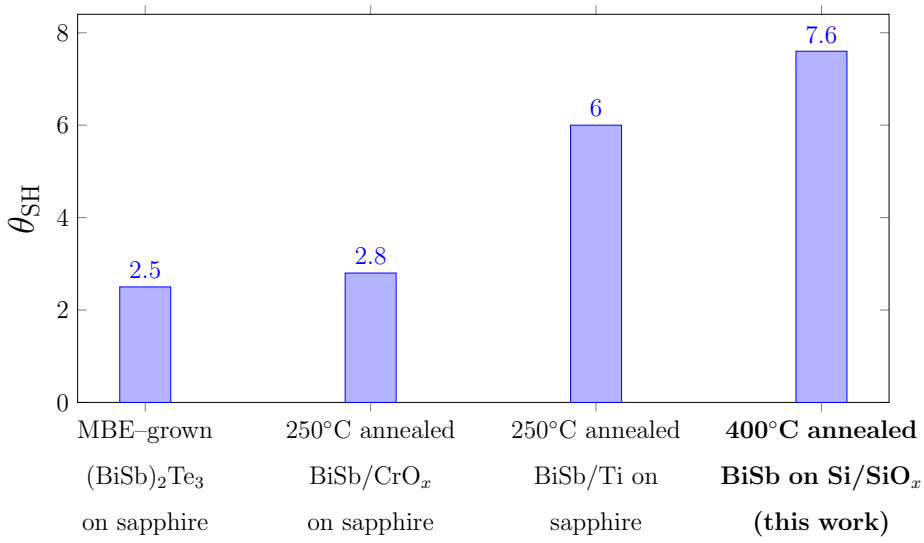

Figure 6.11: Comparison of θ_{SH} from different works.

6.3 Discussion

6.3.1 The limitation of Scherrer equation

Here we explain the large out-of-plane grain size calculated by Scherrer equation in sample A. Scherrer equation assumes that the crystallites are spherical and have a uniform size distribution [16]. BiSb in sample A is likely to have an in-plane grain size that is larger than the total thickness [17], which violates the assumption of Scherrer equation and gives an overestimated out-of-plane grain size. Other techniques, such as TEM, can be used to obtain a highly accurate grain size. However, in this chapter, Scherrer equation can simply provide a qualitative comparison between samples A and B.

6.3.2 The different mechanism of growing BiSb (001) and (012)

In this part, we will discuss the different phases of BiSb between sample A and B. These orientations are likely to be governed by the symmetry and the lattice mismatch of BiSb and the buffer/seed layers. There are several reports on orientation control of BiSb by using different symmetry substrates and buffer layers. For example, the growth mode of BiSb can be either epitaxial (001) or highly-textured (012) [18]. When growing BiSb on GaAs (111) with Ga termination, the threefold symmetry of (111) plane aligns well with BiSb (001), enabling epitaxial growth of high-quality BiSb (001). This process is optimized by cleaning the substrate at high temperatures, then cooling and introducing a GaAs buffer layer before BiSb growth. In another instance, GaAs (111) with As termination creates a more complex reconstruction, which disrupts the epitaxial alignment and typically leads to a textured BiSb (012) orientation. To grow BiSb (012), that work inserted a ultrathin Bi seed layer, which stabilizes the orientation of the subsequent BiSb layer. The Bi seed layer grows in a textured (012) orientation [19], which in turn promotes the (012) alignment of BiSb, despite the asymmetry and reconstruction. However, there are also non-trivial growth modes which do not follow the symmetry matching. On GaAs (001), an unexpected growth mode occurs, where BiSb grows with a textured (001) orientation rather than the (012)

orientation, possibly due to symmetry differences in this four-fold symmetry GaAs (001) compared to hexagonal BiSb (001).

For BiSb fabricated by industrial-friendly sputtering, the single-phase (001) can be promoted on c-plane sapphire substrate with three-fold symmetry [8]. Furthermore, BiSb (012) can be preferrably sputtered on top of an amorphous seed layer and oxidized silicon substrate with local pseudo-hexagonal lattices having approriate lattice matching [20]. This may be the case of our sample A when BiSb was melted and recrystallized into (012) orientation on a thick TiO_x a pseudo-hexagonal lattice that supports four-fold symmetry. In the case of sample B where an additional annealing possibly affected the crystallinity of BiSb, BiSb (001) perhaps was promoted by a pseudo three-fold symmetry of TaO_x with lattice matching similar to the situation of BiSb (001) on c-plane sapphire substrate.

6.3.3 The performance of sample A and B from the viewpoint of thermodynamics

The phase diagram of $Bi_{1-x}Sb_x$ is shown in Figure 6.12 [21, 22]. In this phase diagram, there are four phases marked from I to IV: liquid, mixed state of liquid and solid, solid, and miscibility gap. The miscibility gap is the region that does not exhibit uniform behavior, showing a range between two immiscible layers and two miscible layers [23]. As Sb composition increases, the melting point of BiSb is also risen. In this experiment, we used $Bi_{90}Sb_{10}$ with a melting point approximately 280°C. During the first annealing at 400°C, BiSb exhibited a phase transition from (1) to (2). Consequently, BiSb was melted and its as-growth polycrystalline phase was demolished. After an hour annealing, BiSb was rapidly cooled down by taking the holder away from heat source to room temperature environment at ultrahigh vacuum as depicted from (2) to (1). This process may include the thermodynamic behaviour of the phase transition and phase decomposition. First, BiSb exchanges heat with the environment to lower Gibb free energy and convert back to the equilibrium state in solid phase [24]. When reaching the solid equilibrium, another process of phase separation may happen to determine the homogeneity of the mixing of Bi and Sb. This process is usually

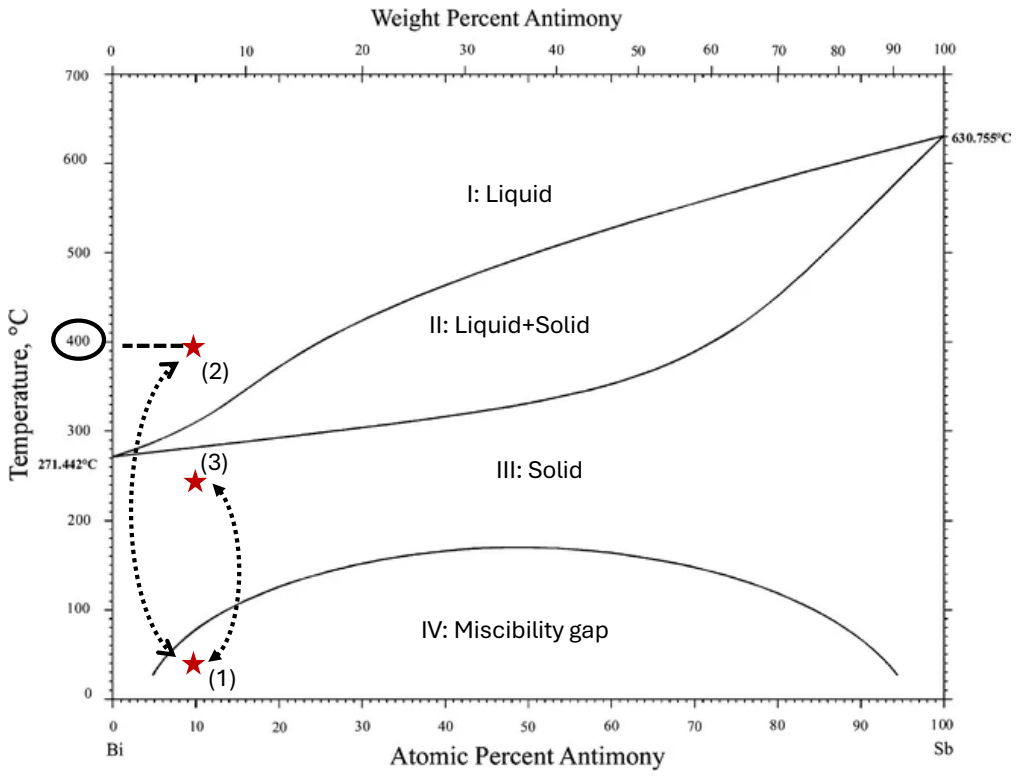

Figure 6.12: Phase diagram of BiSb. Image reproduced with permission of the rights holder Springer Nature.

governed by the Helmholtz free energy F of the system [25]. If the mixed state is highly unstable near the region $\partial^2 F/\partial x^2 < 0$, a spontaneous spinodal decomposition can occur to lower the free energy. If the mixed state is closed to the locally stable states where $\partial^2 F/\partial x^2 > 0$, random nucleation and growth can decompose the mixture in a binodal decomposition process. By using rapid cooling, it is likely to help prevent phase separation, which results in the inhomogeneousity. When Bi and Sb are not mixed well, there is a possibility that Sb can diffuse out of BiSb region as in Section 2.8.4.3, which degrade intrinsic θ_{SH}. Finally, the local crystal structure formation occurs to further lower the chemical energy to the equilibrium state, which may create the single phase (012) in sample A or single phase (001) in sample B. In sample B where the second annealing was below melting point from (1) to (3), the phase decomposition might be triggered again and created a worse mixing state compared to that in sample A. However, the large spin Hall angle is still observed in sample B likely due to

the fact that the top TSS of BiSb in contact with Ti is well protected. The second harmonic Hall voltage is a product of the pure spin current created from the top surface state while the BiSb conductivity is estimated by including both surface states and bulk contribution. This may account for the low BiSb conductivity but large spin Hall angle in sample B.

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Chapter 7: Conclusion

In this dissertation, we have demonstrated the feasibility of integrating BiSb topological insulator into two magnetic storage devices, i.e., SOT reader for HDD applications and SOT-MRAM.

In Chapter 1, we reviewed the development of computing technology in parallel with the emergence of memory technologies. The demand for AI computing has stimulated the research for new memory technologies with ultralow power consumption, high speed of operation, and ultrahigh bit density.

In Chapter 2, we introduced the fundamentals of the spin-orbit physics and emphasized the charge-to-spin conversion via the SHE and the spin-to-charge conversion via the ISHE in NM materials. Furthermore, we presented TIs and their properties that can provide strong SHE. Finally, we focused on the conductive BiSb TI with giant SHE that can be the spin Hall layer in many memory devices and its recent development.

In Chapter 3, we introduced the sputtering technique and the Hall bar patterning process used to fabricate the devices in this dissertation. We also presented the SQUID, XRR and XRD measurements that were used to characterize the samples.

In Chapter 4, we have demonstrated a proof-of-concept BiSb-based SOT reader. With the use of BiSb as the spin Hall layer, we have achieved an output resistance as large as 1.1 Ω and an extracted giant inverse spin Hall angle of 61. This output value has exceeded the minimum requirement to obtain a SNR of 28 dB for the HDD reader application. With such a large inverse spin Hall angle, our device can produce an output voltage of 15 mV with 9.4 kA/cm^2 even at room temperature. This performance is approximately two-million times stronger than that of the Pt-based SOT reader, which indicates the potential of BiSb

to serve in the SOT reader for beyond 4 Tb/in^2 HDD technologies.

In Chapter 5, we have successfully developed a PMA stack by inserting a CrO_x interfacial layer in between bottom BiSb and the trilayers of Ta/CoFeB/MgO on c-plane sapphire. Our findings provide a strategy to optimize the spin Hall angle and the PMA effective field for ultralow power SOT-MRAM cache memory. The CrO_x layer suppresses Sb diffusion, which can degrade BiSb performance via the intrinsic mechanism while providing a relatively good spin transparency. With a thin CrO_x of 1 nm, a relatively large spin Hall angle of $2.5 \sim 2.8$ can be obtained whereas the thicker CrO_x can enhance the PMA effective field significantly. The latter is suitable for low-level cache memories with long bit retention time related to the strong PMA effective field, while the former devices are promising for high-level cache memories thanks to the large spin Hall angle. Furthermore, we have also demonstrated the SOT magnetization switching by a small current density of 3.1 MA/cm^2 with a pulsewidth of 50 µs, which is an order of magnitude smaller than that in HMs.

In Chapter 6, we have investigated the feasibility of integrating bottom BiSb with a high-temperature process beyond its melting point on an amorphous oxidized silicon substrate. By introducing the combination of a buffer layer of TiO_x, an additional seed layer of TaO_x and a protection layer of Ti, we can anneal BiSb at 400°C in ultrahigh vacuum before sputtering the FM multilayers. The XRD spectra show that BiSb has been melted and recrystallized into a single phase from the as-grown polycrystalline. Furthermore, the transport measurement has shown that we have successfully realized a PMA and a large spin Hall angle up to 7.6. We have also demonstrated SOT magnetization switching with a small current density of only 1.3 MA/cm^2 at 50 µs. This work has proved the capability of integrating BiSb with CMOS electronics using BEOL process, which opens a pathway to realize BiSb-based SOT-MRAM and other magnetic storage applications.

List of publication

Journal Publications

1. Z. Ruixian, **H. H. Huy**, T. Shirokura, P. N. Hai, Q. Le, B. York, C. Hwang, X. Liu, M. Gribelyuk, X. Xu, S. Le, M. Maeda, T. Fan, Y. Tao, H. Takano, "High spin Hall angle in BiSb topological insulator and perpendicularly magnetized CoFeB/MgO multilayers with metallic interfacial layers," *Appl. Phys. Lett.*, vol. 124, 072402, 2024.

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